American National Standard

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for information systems — storage module interfaces

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ANSI X3.91M-1982

American National Standard

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American National Standard for Information Systems — Storage Module Interfaces

Secretariat

Computer and Business Equipment Manufacturers Association

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Abstract

This standard defines stringent mechanical, electrical, and functional requirements for attaching disk drives to their control unit. Superset capabilities are defined as extensions. The resulting interface will facilitate the interconnection of disk drives and the control unit (as part of a storage module subsystem) and thus provide a common interface specification for both controller and drive suppliers.

Foreword

(This Foreword is not a part of American National Standard X3.91M-1982.)

As a result of a member's contribution on device-level interfaces, Technical Committee X3T9 formed an ad hoc group on device-level interfaces in February 1977. This group prepared a report that led to the formation of a new task group, X3T9.3, to develop device-level interface standards.

X3T9.3 reviewed current device level interfaces for magnet disk devices in two broad categories: (1) interfaces used on large mainframe computers and (2) interfaces used on magnetic disk devices made for the Original Equipment Manufacturer (OEM) market. It was apparent that mainframe computer device-level interfaces could not be standardized, since each mainframe computer manufacturer employed a unique interface. In the OEM market, however, an interface used on a class of disks commonly called Storage Module Drive (SMD) had achieved a dominant market position and SMD drives were offered as generic products by a number of magnetic disk manufacturers. This SMD interface, in general, offered a simpler interface with less functionality than typical mainframe interfaces, but also cost less and was already a *de facto* industry standard used by many companies. Formal standardization of all mainframe interfaces, therefore, was judged impractical, but a standard on SMD interfaces appeared both practical and desirable.

An effort was then launched to produce a formal standard for the SMD interface. Work began with a review of a number of SMD drive and control unit specifications supplied by the members of X3T9.3. Although no two manufacturers implemented the interface in exactly the same way in all respects, this resulting SMD standard closely follows the prevailing practice in SMD drives.

This standard provides the requirements for the mechanical, electrical, and functional characteristics of the interface between various types of disk drives and their control units. The objective of the standard is to facilitate the interchange of disk drives between storage module subsystems and provide a uniform design approach for attaching disk drives to their control units. Although the standard will not ensure universal interchangeability, it will simplify equipment design and reduce the changes necessary to accomplish the interchange of drives and control units. Additional operational specifications may be developed to provide for total interchange.
While some products may require modification to meet the requirements of this standard, the conversion costs for the bulk of existing SMD products should be low. Sections 1 and 2 provide the scope and basic definitions. Sections 3 through 5 specify the basic minimum interface; most existing disk drives and control units offer all the features described in these sections. Section 6 covers extensions to the basic interface; in this case, existing products are more varied and, when several different implementations of an extension existed, the committee chose the one it judged the best.

Suggestions for improvement of this standard will be welcome. They should be sent to the Computer and Business Equipment Manufacturers Association, 311 First Street, NW, Suite 500, Washington, D.C. 20001.

This standard was processed and approved for submittal to ANSI by American National Standards Committee on Computers and Information Processing, X3. Committee approval of the standard does not imply that all committee members voted for its approval. At the time it approved this standard, the X3 Committee had the following members:

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Task Group X3T9.3 on Device-Level Interface, which recommended the development of this standard, had the following members:

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Contents

American National Standard for Information Systems — Storage Module Interfaces

1. Scope

This American National Standard provides mechanical, electrical, and functional requirements for the storage module class of interface between disk drives and their respective control units. To obtain total interchangeability of such disk drives, an operational manual should be developed. Neither the operational nor ac-power requirements are part of this standard.

The design of the interface provides the following important features:

(1) Addressability of up to 16 disk drives

(2) Capability for both variable and fixed sector sizes

(3) Capability for daisy-chain or radial configuration of control signals with radial configuration of data signals

(4) Data transfer rates across the interface of up to 10 megabits/second

This standard provides a functional description of the interface lines together with electrical and mechanical requirements.

The mechanical and electrical requirements for the interface are defined in Section 3. Section 4 specifies the logical definition of each signal line. Section 5 develops the timing characteristics of each operation at the drive. Section 6 identifies additional features and defines the implementation of these features. Expository remarks concerning the motivation and development of the standard are contained in the Appendix.

This standard is distinct from a specification in that it delineates a minimum, rather than a specific, set of requirements consistent with compatibility and interchangeability of drives. In this standard, the terms "disk drive," "device," and "drive" are equivalent.

2. Definitions

The terms used in this standard shall be defined as shown in the American National Dictionary for Information Processing, ANSI X3/TR-1-77. Terms not covered in ANSI X3/TR-1-77 are defined below:

asserted. A signal is asserted when it is driven to a "true" or "one" value. Tables 1 and 2 show the signal polarities for the asserted condition for each signal. A signal may be either asserted, negated (the "false" or "zero" value), or in a high impedance state.

enabled. A signal is enabled when it is permitted to actively assert or unassert a signal line. Three-state drivers that are not enabled enter the high impedance state.

original equipment manufacturer (OEM). This term, when applied to disk drives, means a drive that is first built by a disk drive manufacturer, then sold to a system vendor who typically integrates the drive with a computer or control unit, and then resold to an end user. This is distinct from a drive that is built, integrated into a computer system, and sold to an end user all by the same manufacturer.

PLO synchronization. This term means "Phase-Lock-Oscillator synchronization."

rotational position sensing. This is a mechanism for detecting the angular position of a reference point on the media with respect to the recording heads.

stranded conductor. A stranded conductor is a conductor composed of a group of small wires usually twisted or braided together.

three-state. When applied to signal drivers, three-state indicates a device which can be in one of three states:

(1) Driving the signal to the asserted value

(2) Driving the signal to the unasserted or "negated" value

(3) A high impedance state that effectively removes the driver from the signal line

twinax. Twinax is a twisted pair in coaxial configuration.

WRITE splice. This is the point on the media in which the head current is turned on or off during a WRITE sequence

3. Physical Characteristics

Unless otherwise indicated, all values include a ±5% tolerance. Signals are assumed to propagate at 70% the speed of light in all cables.

3.1 Cabling Configuration. The disk drives are connected to a control unit by means of a READ/WRITE cable, a CONTROL cable, and a dc ground cable. Delivery of primary ac power cannot be accomplished on any of these cables and is not described in this standard.

A READ/WRITE cable connects each drive directly to the control unit. Fifteen meters is the maximum length of any READ/WRITE cable. A CONTROL cable can connect each drive directly to the control unit (as in Fig. 1a and 1b) or via other drives in a daisy-chain configuration (as in Fig. 2a and 2b). The cumulative length of the CONTROL cables on a given string shall not exceed 30 meters.

A separate dc ground may be provided. Detailed implementation of this grounding requirement is not a subject of this standard. Refer to manufacturer's recommendations for specific power/ground information.

3.2 Connector Characteristics

3.2.1 CONTROL Cable. Control and status information is exchanged between the drive and a control unit via the CONTROL cable. Pin assignments and signal polarities are defined in Table 1. The signal polarities correspond to the asserted state. All pins are enumerated in Table 1. Essential signals are defined in Section 4. Those signals marked with an asterisk are defined in Section 6.

Either of two cable-connector configurations is acceptable for the CONTROL cable. The first connector type is the 75-pin rectangular connector illustrated in Fig. 3. It is used with round, multiple-twisted-pair cable. The second connector type is the 60-pin, two-row, inline connector illustrated in Fig. 4 and 5. It is used with flat-ribbon, multiple-twisted-pair cable. Characteristics of these cables are described in 3.3.1 and 3.3.2.

To allow for the daisy-chain configuration, each drive shall provide two CONTROL cable connectors, one toward and one away from the control unit. With the exception of PICK, all signals shall be carried through from one connector to the other, as well as connected to internal electronics as appropriate. The unidirectional nature of PICK is defined in 6.3. The transmission-line "stub" in each drive shall not exceed 1 meter in length.

3.2.2 READ/WRITE Cable. READ/WRITE DATA, bit synchronization information, and certain dedicated status lines are exchanged between the drive and a control unit via the READ/WRITE cable. These status lines are enabled regardless of whether the drive is selected. Pin assignments and signal polarities are defined in Table 2. The signal polarities correspond to the asserted state. All pins not defined in Table 2 are reserved for options (see Section 6).

Either of two cable-connector combinations is acceptable for the READ/WRITE cable, although the type must correspond with the type chosen for the CONTROL cable. The first connector type is the 34-pin rectangular connector illustrated in Fig. 6. It is used with round, multiple-twisted-pair cable. The second connector type is the 26-pin, two-row, inline connector illustrated in Fig. 7 and 8. It is used with a flat-ribbon cable containing a ground plane. Characteristics of these cables are described in 3.3.1 and 3.3.2.

Termination of the READ/WRITE cable shall be internal to each control unit and drive according to the electrical requirements of 3.4.3.

3.3 Cable Characteristics. Cables shall be either round, jacketed (twisted-pair or twinax and twisted-pair) or flat-ribbon configurations, depending on the input/output connectors selected. Both will be described under their appropriate sections. Round, jacketed (twisted-pair or twinax and twisted-pair) cable is used with rectangular cable-to-panel connectors and flat-ribbon cable is used with ribbon inline connectors.

3.3.1 Round, Jacketed Cable

3.3.1.1 CONTROL Cable. The round twisted-pair cable, when used, shall consist of 36 twisted pairs, a ground wire, and a shield. Each conductor of the twisted-pairs shall be 24 AWG stranded and shall exhibit a characteristic impedance of 100 ohms ± 10 ohms.

3.3.1.2 READ/WRITE Cable. The round twinax and twisted-pair cable, when used, shall consist of five twinax conductor-pairs, four twisted pairs, and three discrete wires. The twinax conductor pairs shall have a characteristic impedance of 160 ohms ± 16 ohms. The conductor shall be 28 AWG. The four twisted-pairs shall have a characteristic impedance of 100 ohms ± 10 ohms. The conductor for the twisted pairs and the discrete wires shall be 26 AWG.

3.3.2 Flat-Ribbon Cable

3.3.2.1 CONTROL Cable. The flat-ribbon cable, when used, shall consist of 30 twisted-pairs. The conductor of each twisted-pair cable shall be 28 AWG. The characteristic impedance of each pair shall be 100 ohms ± 10 ohms.

3.3.2.2 READ/WRITE Cable. The flat-ribbon cable shall consist of 26 conductor ribbon cables with a ground plane and drain wire. The conductor spacing

Table 1
CONTROL Cable Signal Locations

Signal Name	75-Pin Connector Asserted-State Pin Polarity		Source	60-Pin Connector Asserted-State Pin Polarity	
	–	+		–	+
DEVICE SELECT 0/ (EF BUS 0*)	1	4	CU†	23	53
DEVICE SELECT 1/ (EF BUS 1*)	2	5	CU	24	54
DEVICE SELECT 2/ (EF BUS 2*)	3	7	CU	26	56
DEVICE SELECT 3/ (EF BUS 3*)	8	12	CU	27	57
DEVICE SELECT ENABLE	22	25	CU	22	52
SET CYLINDER (TAG 1)	46	49	CU	1	31
HEAD SET (TAG 2)	48	51	CU	2	32
CONTROL SELECT (TAG 3)	52	55	CU	3	33
RPS (TAG 4)*	47	50	CU	30	60
BUS 0	23	26	CU	4	34
BUS 1	24	27	CU	5	35
BUS 2	28	31	CU	6	36
BUS 3	29	32	CU	7	37
BUS 4	30	33	CU	8	38
BUS 5	34	37	CU	9	39
BUS 6	35	38	CU	10	40
BUS 7	36	39	CU	11	41
BUS 8	40	43	CU	12	42
BUS 9	41	44	CU	13	43
INTERFACE ENABLE	16	20	CU	14	44
INDEX MARK	10	13	Drive	18	48
SECTOR MARK	74	77	Drive	25	55
FAULT	11	14	Drive	15	45
SEEK ERROR	75	78	Drive	16	46
ON CYLINDER	15	18	Drive	17	47
UNIT READY	17	21	Drive	19	49
WRITE PROTECTED	53	56	Drive	28	58
ADDRESS MARK	42	45	Drive	20	50
BUSY (Dual Port)*	67	72	Drive	21	51
PICK*	73	–	Drive	29	
SEQUENCE DISABLE*	76	–	Drive	59	–
					–
Terminator Ground	80	–	–	–	–
Cable Shield	82	–	–	–	–

NOTE: Spare pins on the 75-pin connector: 54, 57–60, 62–65, 68, 70, 71, 79.

*These are optional lines defined in Section 6.

†CU = control unit.

Table 2
READ/WRITE Cable Signal Locations

Signal Name	Pin Polarity (Active) –	+	Shield	Source
Round-Cable (34-Pin Connector) Pin Assignments				
WRITE DATA	A	B	D	CU*
WRITE CLOCK	H	J	E	CU
SERVO CLOCK	M	N	K	Drive
READ DATA	U	V	T	Drive
READ CLOCK	W	X	Y	Drive
SELECTED	DD	BB	–	Drive
SEEK END	AA	CC	–	Drive
INDEX MARK†	EE	HH	–	Drive
SECTOR MARK†	FF	JJ	–	Drive
dc Ground	NN	–	–	CU, Drive
–5 Volts†	MM	–	–	Drive
Cable Shield	–	–	Z	CU, Drive
Flat-Cable (26-Pin Connector) Pin Assignments				
WRITE DATA	8	20	7	CU
WRITE CLOCK	6	19	18	CU
SERVO CLOCK	2	14	1	Drive
READ DATA	3	16	15	Drive
READ CLOCK	5	17	4	Drive
SELECTED	22	9	21	Drive
SEEK END	10	23	–	Drive
INDEX MARK†	12	24	11	Drive
SECTOR MARK†	13	26	25	Drive

NOTE: These signals are not gated with UNIT SELECT.

*CU = Control Units.

†These are optional signals defined in Section 6.

shall be 0.050 inch center-to-center to provide for mass termination. The conductors shall be 28 AWG. The characteristic impedance of any single wire driven against the ground plane shall be 65 ohms.

3.4 Electrical Characteristics

3.4.1 Transmitter. Transmitters are differential, three-state devices; each transmitter circuit consists of a negatively connected NPN current switch. Each side of the differential transmitters shall be capable of sinking 12 milliamperes ± 3 milliamperes in the "ON" state, and shall leak no more than 100 microamperes in the high impedance state. When a drive is selected, its transmitters shall switch differentially according to the polarities shown in Fig. 3 and 4. When a drive is not selected, its CONTROL cable transmitters shall have both outputs in the high impedance state.

3.4.2 Receiver. Each receiver circuit is a differential receiver. Its sensitivity shall be ±25 millivolts and it shall reject common-mode noise of at least ±3 volts on its inputs. Differential voltages of at least ±6 volts and common-mode voltages of at least ±5 volts shall be withstood without damage. Series protection resistors of 470 ohms may be used.

3.4.3 Termination

3.4.3.1 CONTROL Cable. All signal pairs except INTERFACE ENABLE, PICK, and SEQUENCE DISABLE shall be electrically terminated within any control unit or disk drive that does not pass on the CONTROL cable in daisy-chain fashion. Thus, both ends of these signals will be terminated. At each end, both sides of each signal pair shall be connected to ground through a 56-ohm resistor.

Instead of cable termination, the INTERFACE ENABLE signal shall be biased to the negated condition in each drive. This may be accomplished with 20 kilohms to +5 volts from the negative side of the pair and 20 kilohms to -5 volts from the positive side. The termination of PICK and SEQUENCE DISABLE are described in 6.3.

3.4.3.2 READ/WRITE Cable. The READ DATA,

WRITE DATA, SERVO CLOCK, READ CLOCK, and WRITE CLOCK signals shall be terminated with resistors from each side of the differential line to ground at the receiving end only. The resistor values shall be 68 ohms for the flat cable and 82 ohms for the round cable. READ DATA, READ CLOCK, and SERVO CLOCK are terminated in the controller and WRITE DATA and WRITE CLOCK are terminated in the drive.

All other signals remaining in the READ/WRITE cable shall be terminated with 68-ohm (flat-cable) or 56-ohm (round-cable) resistors from each side of the differential line to ground at the receiver end.

3.4.4 Cable Lengths. The transmitting and receiving circuitry shall function properly with READ/WRITE cable lengths of up to 15 meters and with cumulative CONTROL cable chain lengths of up to 30 meters.

4. Signal Definitions

This section defines essential signals and the intended operation and states of the signals. Relative signal timings and tolerances are defined in Section 5.

4.1 CONTROL Cable Interface. Control and status information is exchanged between a drive and a control unit via the CONTROL cable. Pin assignments and signal polarities are defined in Table 1.

4.1.1 Output Lines (Control Unit to Drive). There are 20 output lines between the control unit and the drive. They are as follows:

1 DEVICE SELECT ENABLE
4 DEVICE SELECT
1 INTERFACE ENABLE
4 Function tags
10 BUS-OUT lines

4.1.1.1 Device Selection Lines. These lines are used for the logical connection of a disk drive to the control unit.

4.1.1.1.1 DEVICE SELECT 3, 2, 1, 0. These four lines are decoded to select one of up to sixteen drives on the CONTROL cable. DEVICE SELECT 3, 2, 1, and 0 correspond to binary weights 8, 4, 2, and 1, respectively, when specifying the select number. The select number is determined by the drive. Each drive on a given CONTROL cable chain shall have a unique select number.

4.1.1.1.2 DEVICE SELECT ENABLE. Selection of the drive occurs at the leading edge of DEVICE SELECT ENABLE provided that the select number on the DEVICE SELECT lines is equal to that designated within the drive. Selection of the drive is acknowledged by the assertion of SELECTED on the READ/WRITE cable. The drive will remain selected until DEVICE SELECT ENABLE is negated. The drive will acknowledge deselection by negating SELECTED. If either the drive's select number or the DEVICE SELECT lines are changed while the drive is selected, the drive will remain selected and responsive to the control unit until SELECT ENABLE is dropped by the control unit.

4.1.1.2 INTERFACE ENABLE (or OPEN CABLE DETECT). This signal, when asserted, enables the drive's receivers and drivers and allows selection and operation of the drive from the control unit. Negation of this signal will disable the drive's receivers and drivers. During the entire control unit's internal power sequencing (up or down), this signal shall be negated to prevent spurious information transfer. The INTERFACE ENABLE signal is terminated in such a way that removal of the cable will disable line receivers.

4.1.1.3 Function Tags. These tags, asserted singly, perform the following operations on a selected disk drive (see Tables 1 and 2).

4.1.1.3.1 SET CYLINDER. This tag line transfers the cylinder address bits to the drive via BUS lines. BUS 9, 8, . . . , 0 correspond to binary weights 512, 256, . . . , 1, respectively, when determining the cylinder address.

If the cylinder address is invalid, SEEK ERROR is asserted in response to the leading edge of SET CYLINDER. ON CYLINDER and SEEK END are always negated on the trailing edge of SET CYLINDER.

4.1.1.3.2 HEAD SET. This command transfers the head address bits to the drive via the BUS lines. BUS lines 6, 5, . . . , 0 correspond to binary weights 64, 32, . . . , 1, respectively, when determining the head address. The head address specifies one of the tracks on a given cylinder on which READ or WRITE operations may be performed. Note that the number of heads is drive dependent.

4.1.1.3.3 CONTROL SELECT. This signal, when active, allows the BUS lines to control operations in a selected drive. The significance of the BUS lines with the CONTROL SELECT asserted is as follows:

(1) BUS 0 – WRITE GATE. With ADDRESS MARK ENABLE negated, WRITE GATE command enables the write circuitry to transfer the serialized information on the WRITE DATA line to the recording medium. If ADDRESS MARK ENABLE is asserted during WRITE GATE, the drive will record an address mark. While the WRITE GATE is asserted, the drive faults related to WRITE operations may be detected and signaled via the FAULT line on the CONTROL cable.

Other than ADDRESS MARK ENABLE, all other combinations of control functions asserted with WRITE GATE result in undefined action.

(2) BUS 1 – READ GATE. With ADDRESS MARK ENABLE negated, READ GATE command enables the read circuitry to transfer the serialized information on the READ DATA line from the recording medium. If ADDRESS MARK ENABLE is asserted during READ GATE, the drive will search for a previously recorded address mark.

NOTE: The READ GATE must be asserted while the read head is positioned over a zero data field area of the track for proper synchronization. See manufacturer's specification for exact timing.

Any combination of the following conditions may also be asserted:

(a) ADDRESS MARK ENABLE

(b) OFFSET FORWARD or OFFSET REVERSE, but not both

(c) DATA STROBE EARLY or DATA STROBE LATE, but not both

All other combinations of control functions asserted with READ GATE result in undefined action.

(3) BUS 2 – OFFSET FORWARD. Assertion of the OFFSET FORWARD command displaces the head positioner a fixed amount, from its normal position towards the spindle center. The leading edge of this command causes the negation of ON CYLINDER during the offset positioning in conjunction with SEEK END. The trailing edge of OFFSET FORWARD initiates the removal of the offset condition.

Any combination of the following signals may also be asserted:

(a) READ GATE

(b) ADDRESS MARK ENABLE

(c) DATA STROBE EARLY or DATA STROBE LATE, but not both

(d) FAULT RESET

All other combinations of control functions asserted with OFFSET FORWARD result in undefined action.

NOTE: This command, if asserted during WRITE GATE, causes the assertion of FAULT.

(4) BUS 3 – OFFSET REVERSE. Identical to the OFFSET FORWARD command, but displaces the head positioner in the opposite direction.

(5) BUS 4 – FAULT RESET. This signal clears the FAULT status provided no condition remains that activates FAULT. REZERO, RELEASE, or both may also be asserted. All other combinations of control functions asserted with FAULT RESET result in undefined action.

(6) BUS 5 – ADDRESS MARK ENABLE. This command, used only for variable sector formats, allows the control unit to record and identify record boundaries. When asserted in conjunction with WRITE GATE, the drive records an address mark. This command, when used in conjunction with READ GATE, causes the drive to assert ADDRESS MARK when a previously recorded address mark is detected.

The following conditions may also be asserted:

(a) WRITE GATE

(b) READ GATE

READ GATE may be asserted with OFFSET FORWARD or OFFSET REVERSE and DATA STROBE EARLY or DATA STROBE LATE. Both OFFSET signals and both DATA STROBE signals shall not be used simultaneously. READ GATE may be asserted by itself.

All other combinations of control functions asserted with ADDRESS MARK ENABLE result in undefined action.

(7) BUS 6 – REZERO. This command causes the head positioner to reposition to cylinder 0 and resets the head address register to zero. The leading edge of REZERO negates ON CYLINDER, SEEK END, and SEEK ERROR. FAULT RESET, RELEASE, or both may also be asserted. All other combinations of control functions asserted with REZERO result in undefined action.

(8) BUS 7 – DATA STROBE EARLY. During assertion of the DATA STROBE EARLY command, the drive's internal data recovery logic will strobe the READ data at a time earlier than normal. The normal stroke timing and the timing charge covered by this signal are drive dependent.

Any combination of the following commands may also be asserted:

(a) READ GATE

(b) ADDRESS MARK ENABLE

(c) OFFSET FORWARD or OFFSET REVERSE, but not both

All other combinations of control functions asserted with DATA STROBE EARLY result in undefined action.

(9) BUS 8 – DATA STROBE LATE. During assertion of the DATA STROBE LATE command, the drive's internal data recovery logic will strobe the READ data at a time later than normal. In all other respects, this command is identical to DATA STROBE EARLY.

(10) BUS 9 – Not Used. This signal is not used when CONTROL SELECT is asserted.

4.1.1.3.4 ROTATIONAL POSITION SENSING (RPS). The use of this signal is optional. It is defined in 6.4.

4.1.2 Input Lines (Drive to Control Unit). There are 8 status lines between the drive and control unit that serve as input lines. They are as follows:

(1) INDEX MARK

(2) SECTOR MARK

(3) FAULT
(4) SEEK ERROR
(5) ON CYLINDER
(6) UNIT READY
(7) WRITE PROTECTED
(8) ADDRESS MARK

NOTE: If the drive has a maintenance mode, and the mode is activated, all output lines will be ignored and all input lines will be held inactive.

The drive shall be selected to enable the following status lines onto the BUS line.

4.1.2.1 INDEX MARK. This status line, when asserted, indicates that the reference point or index area is passing under the heads. This pulse occurs once per revolution of the recording surface.

4.1.2.2 SECTOR MARK. This status line establishes rotational reference points on the recording surface. Each track may be divided into sectors with the initial sector starting coincident with the INDEX MARK. SECTOR MARK is omitted at the initial sector. SECTOR MARK indicates the beginning of each subsequent sector. The number of sectors into which each track is divided is determined within the drive.

4.1.2.3 FAULT. When asserted, this line indicates that a fault condition (for example, READ/WRITE unsafe) has occurred within the drive. The FAULT condition disables the READ and WRITE operations within the drive. This condition also causes negation of UNIT READY (ON CYLINDER and SEEK END remain unaffected). The FAULT signal is reset either by a FAULT RESET command, or optionally by operator intervention at the drive, provided no condition remains that activates FAULT.

4.1.2.4 SEEK ERROR. When asserted, this status line indicates that the drive failed to complete an initial head load, SET CYLINDER, or REZERO command. SEEK ERROR also results when an invalid cylinder address is received by the drive. The SEEK ERROR status may be negated either by a REZERO command from the control unit or optionally by operator intervention at the drive.

4.1.2.5 ON CYLINDER. This status line indicates that the heads are stabilized at a usable cylinder. However, ON CYLINDER is not negated when OFFSET FORWARD or OFFSET REVERSE is removed. ON CYLINDER is negated on the trailing edge of the SET CYLINDER command or on the leading edge of REZERO, OFFSET FORWARD, or OFFSET REVERSE.

4.1.2.6 UNIT READY. This status line indicates that the drive is ready to accept commands and that no FAULT condition exists within the drive.

4.1.2.7 WRITE PROTECTED. This line indicates that recording of information on the recording surface is inhibited at the drive. Asserting WRITE GATE after WRITE PROTECTED has been asserted causes FAULT to be asserted.

4.1.2.8 ADDRESS MARK. This line indicates drive detection of a previously recorded address mark, when READ GATE and ADDRESS MARK ENABLE are both asserted.

4.2 READ/WRITE Cable Interface. The READ/WRITE cable signals are listed in Table 2. Signals on this cable are continuously available when the drive is powered on.

4.2.1 WRITE CLOCK. The WRITE CLOCK is used by the drive to strobe the WRITE DATA line while recording. WRITE CLOCK is generated in the control unit by regenerating the drive's SERVO CLOCK signal. The WRITE CLOCK signal shall precede and be transmitted continuously during the assertion of WRITE GATE.

4.2.2 WRITE DATA. The WRITE DATA line carries the serial data to the drive during WRITE GATE assertion. The serial write data is strobed with the WRITE CLOCK.

4.2.3 SERVO CLOCK. The SERVO CLOCK is developed within the drive and provides the control unit a reference clock that synchronizes WRITE DATA to the rotational position of the recording surface during a WRITE operation. The SERVO CLOCK is valid only when UNIT READY is asserted.

4.2.4 READ CLOCK. The READ CLOCK signal is developed within the drive. The leading edge of the READ CLOCK signal is used by the control unit to strobe READ DATA.

4.2.5 READ DATA. The READ DATA line carries serial data synchronized with READ CLOCK during the assertion of READ GATE.

4.2.6 SELECTED. This signal is transmitted from the drive to the control unit to indicate successful selection of a device. SELECTED will remain asserted until DEVICE SELECT ENABLE is negated.

4.2.7 SEEK END. This signal is asserted in response to the assertion of either ON CYLINDER or SEEK ERROR. SEEK END is negated as a result of the assertion of SET CYLINDER or the negation of UNIT READY.

5. Timing Characteristics

The timing characteristics described in the following paragraphs are referenced to the signals at the drive interface connector. The control unit timing should be designed to accommodate cable delays and signal skew within the cables.

5.1 Device Selection Sequence. The timing for the initial selection of a drive is defined by Fig. 9. The control unit should wait a delay of at least 1 microsecond following the assertion of DEVICE SELECT ENABLE before sampling the status and selected lines. Since the SELECTED signal is in a separate cable from the status lines, it should not be used to strobe the status lines. The timing for device deselection is defined by Fig. 10.

5.2 SEEK Command Sequence. The timing for a SEEK command with a valid moving head cylinder number is defined by Fig. 11a. If the BUS lines contain an invalid moving head cylinder address the timing is defined by Fig. 11b.

5.3 REZERO Command Sequence. The timing for a REZERO command is defined by Fig. 12.

5.4 OFFSET Command Sequence. The OFFSET command timing is defined by Fig. 13. When an OFFSET command is negated, a delay of at least 10 milliseconds must be guaranteed by the control unit prior to assertion of SEEK, REZERO, READ, or WRITE commands.

5.5 HEAD SET Command Sequence. The timing for a HEAD SET command is defined by Fig. 14.

5.6 FAULT CLEAR Command Sequence. The timing for a FAULT CLEAR command is defined by Fig. 15. If the fault is permanent, the fault status will not reset as a result of the FAULT CLEAR command.

5.7 INDEX MARK and SECTOR MARK Timing. The INDEX MARK is a pulse with a 2.0 microsecond minimum duration. The SECTOR MARK is a pulse with a 1.0 microsecond minimum duration. The maximum duration of either pulse shall be 5.0 microseconds. The drive inhibits the SECTOR pulse during the INDEX pulse so that a SECTOR pulse is not transmitted at INDEX. The INDEX and SECTOR status lines are enabled by DEVICE SELECT, thus the control unit shall ignore the INDEX MARK and SECTOR MARK lines for at least 5.0 microseconds from the time that the status lines are valid to ensure a valid INDEX or SECTOR pulse.

5.8 READ Command Sequence. The timing for the READ command sequence is defined by Fig. 16. Data shall be recovered correctly if the READ GATE command is asserted in a field of zeros that lasts after READ GATE for the PLO synchronization interval.

To ensure the recovery of previously recorded data, the following timing requirements shall be satisfied by the control unit and the track format.

5.8.1 SEEK END (ON CYLINDER) to READ GATE. The assertion of READ GATE shall occur a minimum of 500 nanoseconds following the assertion of SEEK END or ON CYLINDER.

5.8.2 OFFSET to READ GATE. The assertion of the READ GATE command shall occur a minimum of 10 milliseconds following the negation of an OFFSET FORWARD or OFFSET REVERSE command.

5.8.3 HEAD SET to READ GATE. The assertion of READ GATE command shall occur a minimum of 25 microseconds following the negation of the HEAD SET command.

5.8.4 WRITE GATE to READ GATE. The assertion of READ GATE shall occur a minimum of 30 microseconds following the negation of the WRITE GATE command.

5.9 WRITE Command Sequence. The timing for the WRITE command sequence is defined by Fig. 17. A WRITE command sequence shall be initiated immediately following a WRITE ADDRESS MARK or READ ADDRESS MARK command sequence.

To ensure storage of data for subsequent recovery, a WRITE sequence shall begin with a synchronization field of zeros. The following timing requirements shall be satisfied by the control unit and track format.

5.9.1 SEEK END (ON CYLINDER) to WRITE GATE. The assertion of the WRITE GATE command shall occur a minimum of 500 nanoseconds following the assertion of an ON CYLINDER or SEEK END status.

5.9.2 OFFSET to WRITE GATE. The assertion of the WRITE GATE command shall occur a minimum of 10 milliseconds following the negation of either an OFFSET FORWARD or an OFFSET REVERSE command.

5.9.3 HEAD SET to WRITE GATE. The assertion of the WRITE GATE command shall occur a minimum of 5 microseconds following the negation of the HEAD SET command.

5.9.4 READ GATE to WRITE GATE. The assertion of WRITE GATE shall occur a minimum of 500 nanoseconds following the negation of the READ GATE command.

5.10 READ ADDRESS MARK Command Sequence. The timing for the READ ADDRESS MARK command sequence is defined by Fig. 18. The same figure defines the ADDRESS MARK FOUND pulse duration. This pulse duration is not affected by the negation of the READ ADDRESS MARK command.

To ensure recovery of an ADDRESS MARK, the following timing requirements shall be satisfied by the control unit and the track format.

5.10.1 SEEK END to READ ADDRESS MARK. The assertion of the READ ADDRESS MARK com-

mand shall occur a minimum of 500 nanoseconds following the assertion of ON CYLINDER or SEEK END status.

5.10.2 OFFSET to READ ADDRESS MARK. The assertion of the READ ADDRESS MARK command shall occur a minimum of 10 milliseconds following the negation of either an OFFSET FORWARD or an OFFSET REVERSE command.

5.10.3 HEAD SET to READ ADDRESS MARK. The assertion of the READ ADDRESS MARK command shall occur a minimum of 20 microseconds following the negation of the HEAD SET command.

5.10.4 WRITE GATE to READ ADDRESS MARK. The assertion of the READ ADDRESS MARK command shall occur a minimum of 25 microseconds following the negation of the WRITE GATE command.

5.10.5 READ GATE to READ ADDRESS MARK. The assertion of the READ ADDRESS MARK command shall occur a minimum of 500 nanoseconds following the assertion of the READ GATE command.

5.11 WRITE ADDRESS MARK Command Sequence. The timing for the WRITE ADDRESS MARK command is defined by Fig. 19. WRITE GATE precedes ADDRESS MARK ENABLE and shall meet all requirements of 5.9.

To ensure generation of an ADDRESS MARK for subsequent recovery, the following timing requirements shall be satisfied by the control unit and the track format.

5.11.1 SEEK END (ON CYLINDER) to WRITE ADDRESS MARK. The assertion of the WRITE ADDRESS MARK command shall occur a minimum of 500 nanoseconds following the assertion of the SEEK END or ON CYLINDER status.

5.11.2 OFFSET to WRITE ADDRESS MARK. The assertion of the WRITE ADDRESS MARK command shall occur a minimum of 10 milliseconds following the negation of either an OFFSET FORWARD or an OFFSET REVERSE command.

5.11.3 HEAD SET to WRITE ADDRESS MARK. The WRITE ADDRESS MARK command shall occur a minimum of 5 microseconds following the negation of the HEAD SET command.

5.12 SERVO CLOCK. This clock has a duty cycle of 50% ± 3%.

5.13 READ CLOCK and READ DATA. The READ CLOCK and READ DATA signals shall be synchronized as defined by Fig. 20.

5.14 WRITE CLOCK and WRITE DATA. The WRITE CLOCK and WRITE DATA signals shall be synchronized as defined in Fig. 21.

6. Interface Extensions

The storage module interface defined by Sections 3, 4, and 5 form the basic equipment covered by this standard. Compliance with this standard requires that all of the features described in Sections 3, 4, and 5 be implemented in the manner specified. This section describes extensions to the basic equipment that may be optionally added in any control-unit/drive design. Whenever any of these extensions are included, conformance to this standard requires that they be implemented in the manner specified.

All signals returned by the drive to a control unit function as described in Section 4 unless indicated otherwise in this section.

6.1 Extended Functions. The lines SET CYLINDER, HEAD SET, CONTROL SELECT, and ROTATIONAL POSITION SENSING (RPS) are also named TAG 1, TAG 2, TAG 3, and TAG 4, respectively. These lines will be referred to as the TAG N lines for this subsection.

The existing cable configuration limits the number of available signal lines. To increase the information flow between control unit and drive, a bidirectional BUS line and an extended function (EF) BUS line are defined. Bidirectional BUS lines may be driven by either the control unit and the drive, but not by both simultaneously (see Fig. 22).

Device selection number and the EF BUS share the same four lines (see Table 1). The leading edge of DEVICE SELECT ENABLE selects the drive. From this point until the device deselection sequence (see Fig. 10), these lines function as the EF BUS.

The EF BUS lines specify one of sixteen combinations, modifying the actions taken when TAG 1, 2, 3, or 4 is asserted. TAG 3 with EF BUS = 0 specifies the CONTROL SELECT operation.

The directionality of the BUS lines is thus determined by the state of the TAG N and EF BUS lines.

The drive shall contain a means to disable the EF BUS, allowing the drive to operate with control units not implementing this extension.

6.2 Dual Port. The dual port extension allows interleaved access to one drive by two control units. The dual port operates as a switch that routes control, data, and status signals between the drive and the control unit to which the drive may be reserved. Once selection is accomplished, the dual port is not apparent to normal operation of the interface.

The dual port interface communicates with the two control units through two identical interfaces designated Port A and Port B. The physical interface between each port and its attached control unit consists

of a READ/WRITE cable and a CONTROL cable with provisions for daisy chaining or terminating the CONTROL cable (see Fig. 23).

6.2.1 Signal Descriptions

6.2.1.1 BUSY. This signal is enabled by the drive onto the CONTROL cable when that drive is selected. It is asserted if the drive is reserved to the other control unit, and negated otherwise.

BUSY -	67 (Round Cable)	21 (Flat Cable)
BUSY +	72 (Round Cable)	51 (Flat Cable)

6.2.1.2 SEEK END. While a drive is reserved to one control unit, SEEK END is asserted to the nonreserving control unit. If the drive is reserved by one control unit and selection is attempted by the other control unit during the period of reservation, SEEK END is negated to the nonreserving control unit for a period of 30 microseconds after the reserving control unit releases the drive.

6.2.2 Device Reservation and Release

6.2.2.1 Reservation. The drive becomes reserved to a control unit when it is selected by that control unit and not already reserved by the other control unit. It remains reserved until released, or until a PRIORITY SELECT command sequence occurs on the other port. On power-up, the drive is not reserved to either control unit.

If the drive was reserved by the first control unit and selection was attempted by the second control unit during the period of reservation, the drive becomes reserved to the second control unit after the first control unit releases the drive.

6.2.2.2 PRIORITY SELECT Command Sequence. Drive reservation will be forced from one control unit to another if the control unit demanding reservation performs a PRIORITY SELECT command sequence consisting of a unit selection sequence with BUS 9 asserted. Drive reservation is switched at the leading edge of SELECT ENABLE. Continued assertion of BUS 9 and SELECT ENABLE by that control unit does not prevent the other control unit from reserving the drive by issuing a PRIORITY SELECT command sequence.

6.2.2.3 UNIT RELEASE. The drive will be released by the control unit if the control unit asserts CONTROL SELECT and BUS 9 while the drive is selected. The drive remains reserved until SELECT ENABLE is negated. FAULT RESET, REZERO, or both can also be asserted. All other combinations of control functions asserted with UNIT RELEASE result in undefined action.

6.2.2.4 Release Timer. The drive may be released by a timer 500 milliseconds after it was last reserved, or after its reservation is changed from one port to the other. A means should be provided to inhibit the release timer. The states are:

(1) Inhibit: The drive stays reserved to a control unit until that control unit issues a RELEASE command sequence, the other control unit issues a PRIORITY SELECT command sequence, or the drive is powered down.

(2) Enable: The reserve timer releases the drive 500 milliseconds after the last reservation.

6.2.2.5 Simultaneity. In the event of simultaneous occurrence, the order of precedence shall be PRIORITY SELECT B over PRIORITY SELECT A over RELEASE B over RELEASE A over the timer.

6.3 Spinup Sequencing. Drive spinup sequencing is controlled by the lines PICK and SEQUENCE DISABLE (see Fig. 24). These are single-ended lines as defined in a string; PICK IN is defined as PICK from the control unit direction. Likewise, PICK OUT is defined as PICK away from the control unit. PICK is passed on in such a manner that PICK OUT of one drive connects to PICK IN of the next drive in the string. PICK IN to the first drive in the string is controlled by the control unit. SEQUENCE DISABLE is controlled by any drive in the process of spinning up.

A drive begins its spinup sequence only if its power is on, its start switch is enabled, PICK IN is asserted (grounded) on either port, and SEQUENCE DISABLE is negated (high) on the same port. The control unit and each drive shall be capable of sinking 60 milliamperes when PICK is asserted. The drive may not pull up PICK more than +20 volts. SEQUENCE DISABLE is biased at the control unit by a 2200-ohm resistor to +5 volts. While spinning up, a drive asserts SEQUENCE DISABLE on both ports, and negates PICK OUT from both ports. When it has spun up, it releases SEQUENCE DISABLE on both ports and asserts PICK OUT from either port that has PICK IN asserted. The assertion level of SEQUENCE DISABLE is 5.5 volts maximum.

Each unit propagates PICK IN to PICK OUT if its start switch is disabled, if it is not powered up, or if its spinup sequence is complete. A drive shall receive PICK IN for a minimum of 10 milliseconds before beginning a spinup sequence. A drive shall spin up and propagate PICK IN a maximum of 1 minute. The control unit shall maintain PICK for the sum of the spinup propagation times of the drives attached to it.

Negation of INTERFACE ENABLE for a minimum of 50 milliseconds constitutes a spindown command.

6.4 ROTATIONAL POSITION SENSING (TAG 4). The assertion of TAG 4 transfers the sector address on the BUS lines to the drive (see Fig. 25). SEEK END is

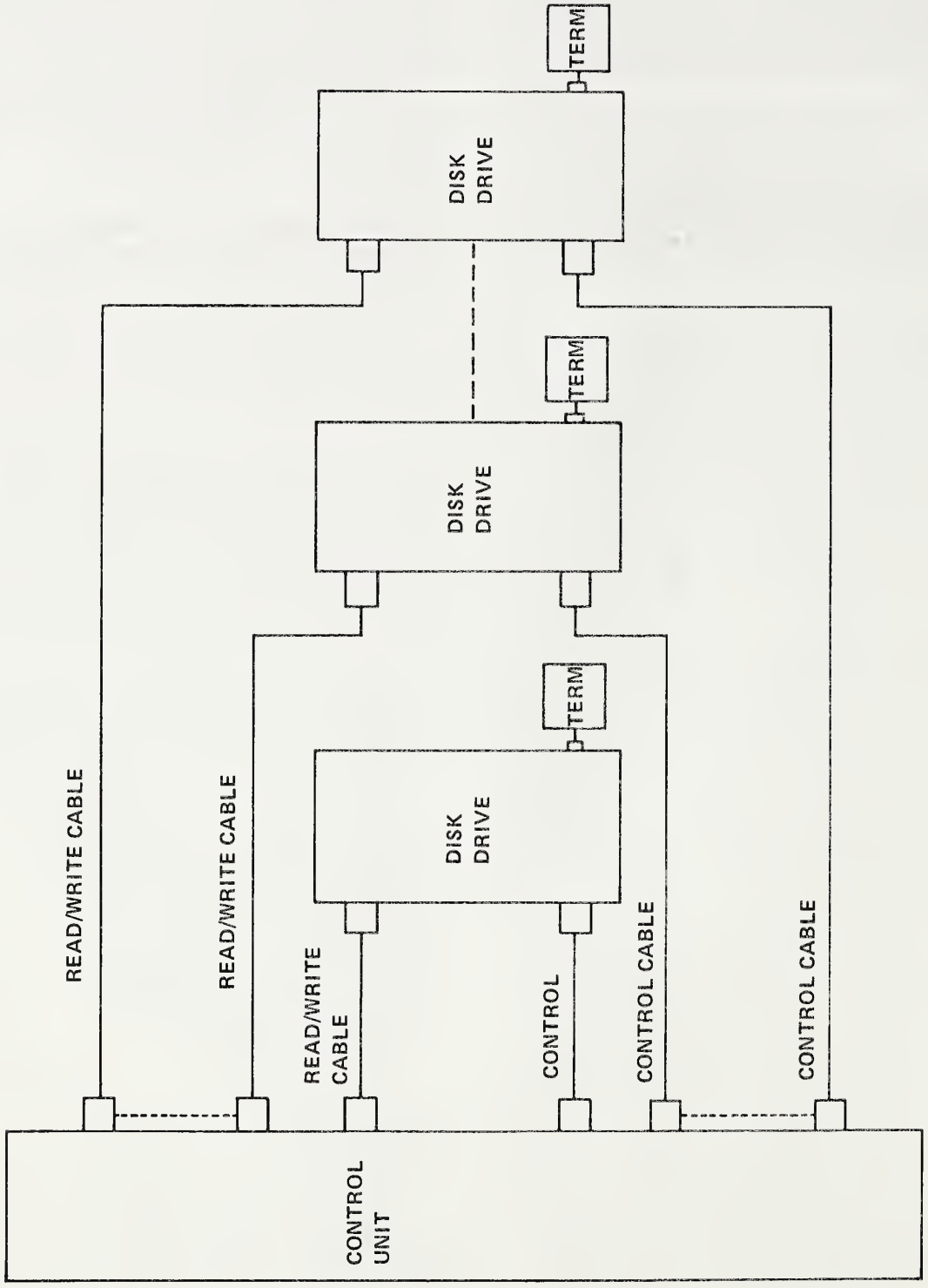
asserted with ON CYLINDER while the sector address that was last transmitted by RPS compares with the address of the sector passing under the heads. SEEK END is then asserted once per revolution, while the sector address compares, until the drive is selected. SEEK END is also asserted in the case of SEEK ERROR.

RPS -	47 (Round Cable)	30 (Flat Cable)
RPS +	50 (Round Cable)	60 (Flat Cable)

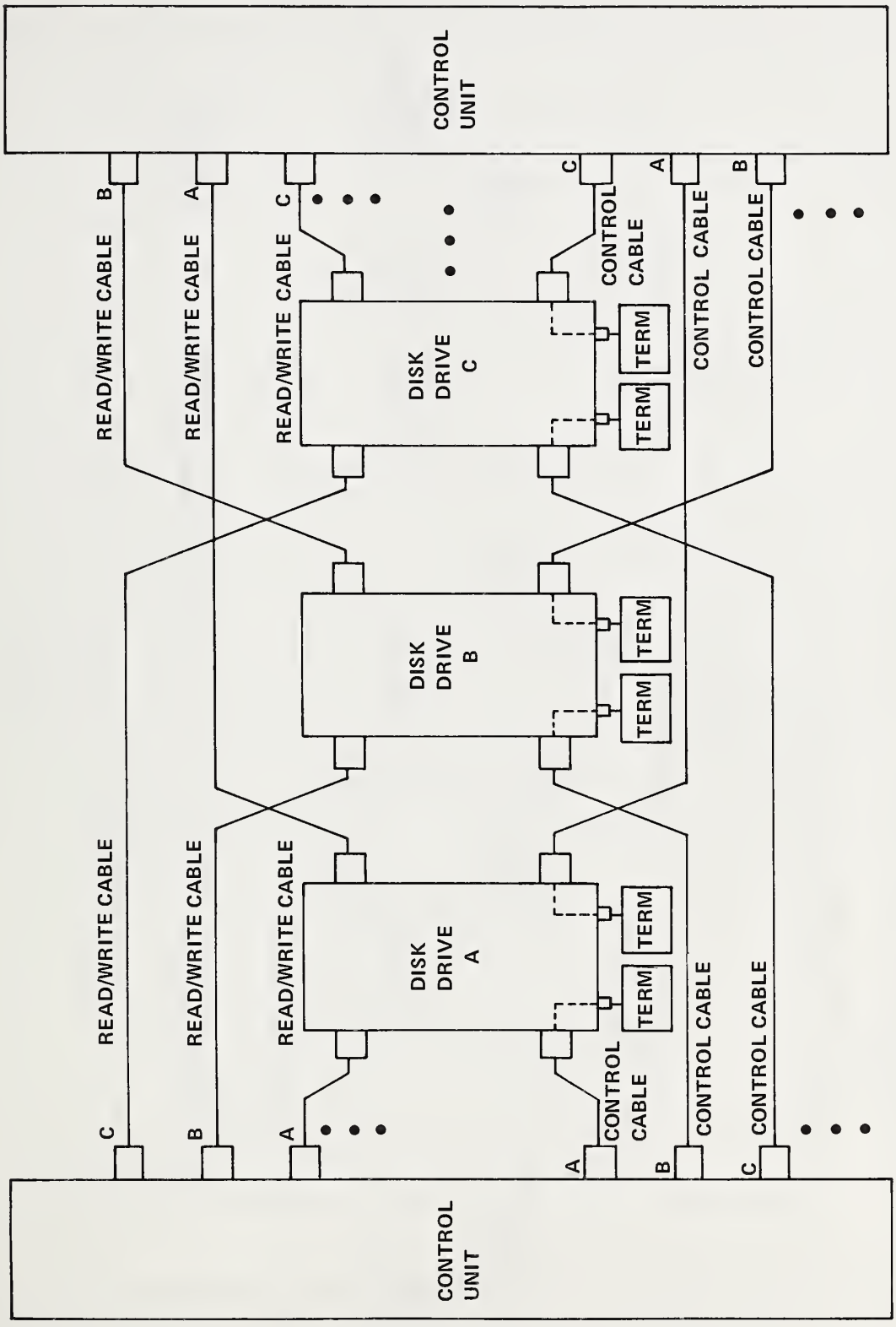
6.5 INDEX MARK and SECTOR MARK. These lines are available on the READ/WRITE cable and are not gated by UNIT SELECT. See 4.1.2.1 and 4.1.2.2 for definitions of these status lines.

6.6 Fixed-Head Addressing. The fixed-heads in a drive are addressed as a unit number that may, at the user's option, be distinct from the unit number that addresses the moving-head address space in a drive. The fixed-heads are organized within that unit as a contiguous set of cylinders with the same number of tracks per cylinder as the moving-head address space. ON CYLINDER and SEEK END refer only to the status of the moving-head positioner, even if the fixed-heads are addressed.

6.7 Service Voltages on Round Radial Cable. Some service equipment requires -5 volts on pin MM of the round cable.



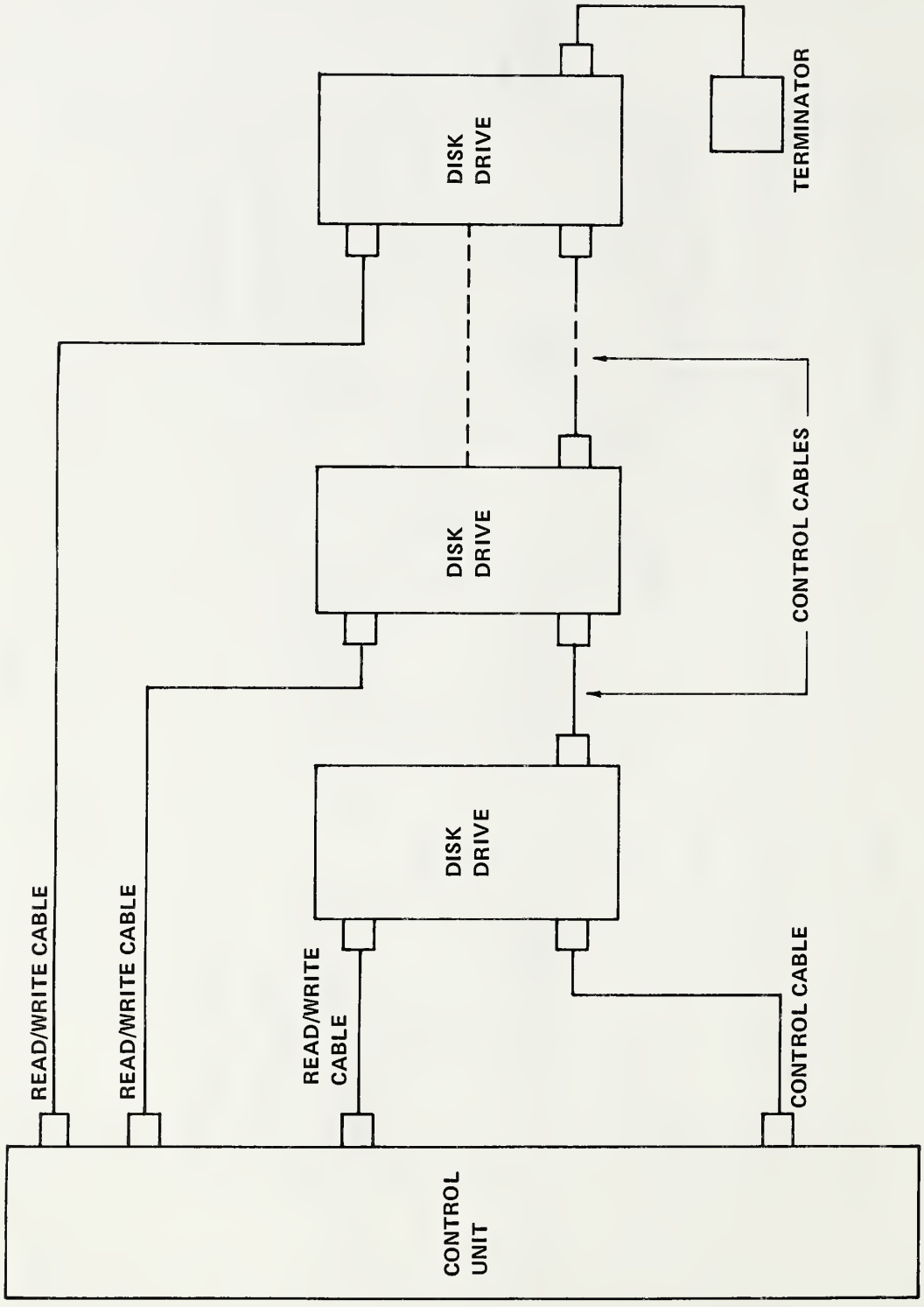
(a) Single Port



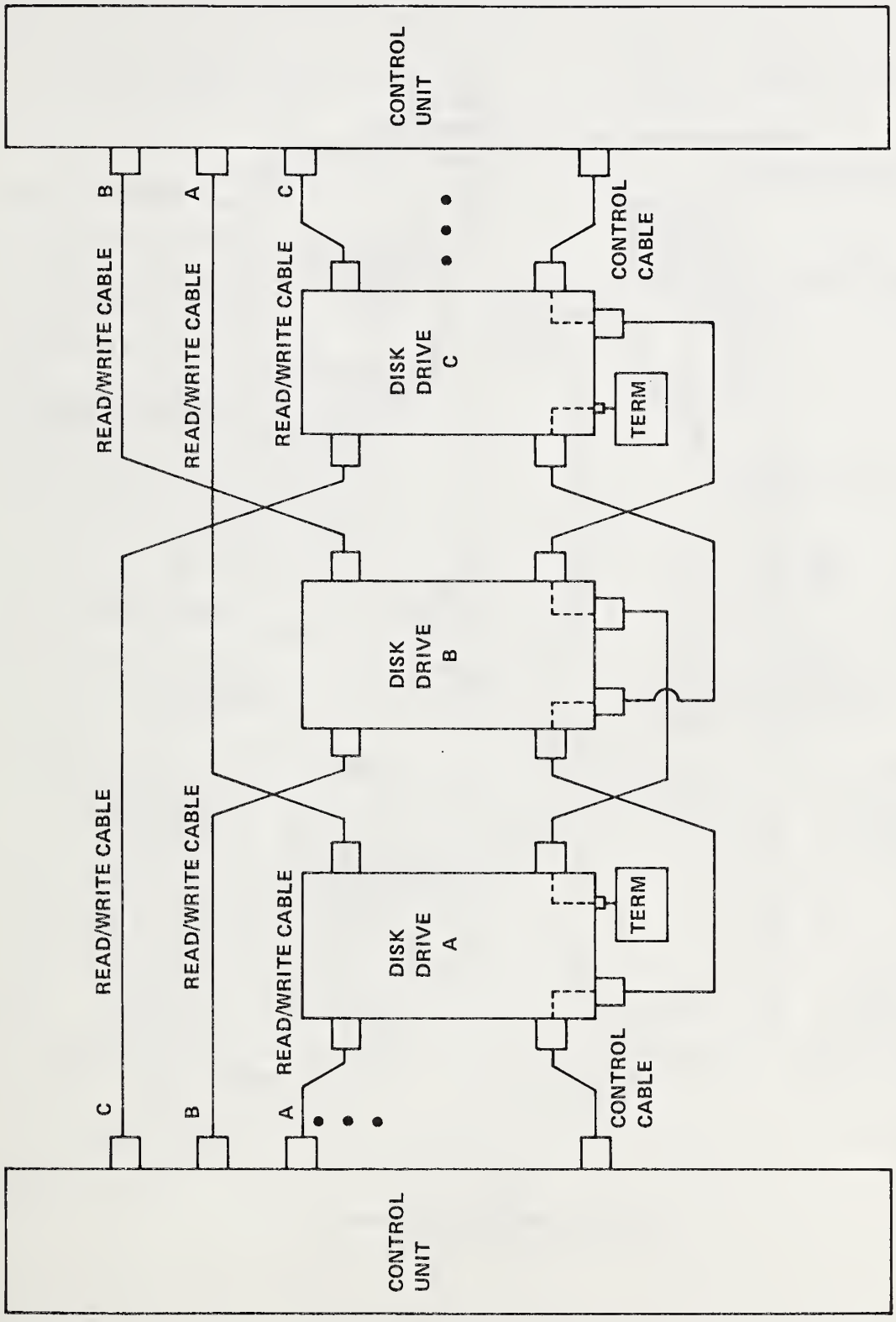
(b) Dual Port

NOTE: Optional configuration defined in Section 6.

Fig. 1
Radial Cabling Configuration



(a) Single Port



(b) Dual Port

Fig. 2
Daisy-Chain Cabling Configuration

NOTE: Optional configuration defined in Section 6.

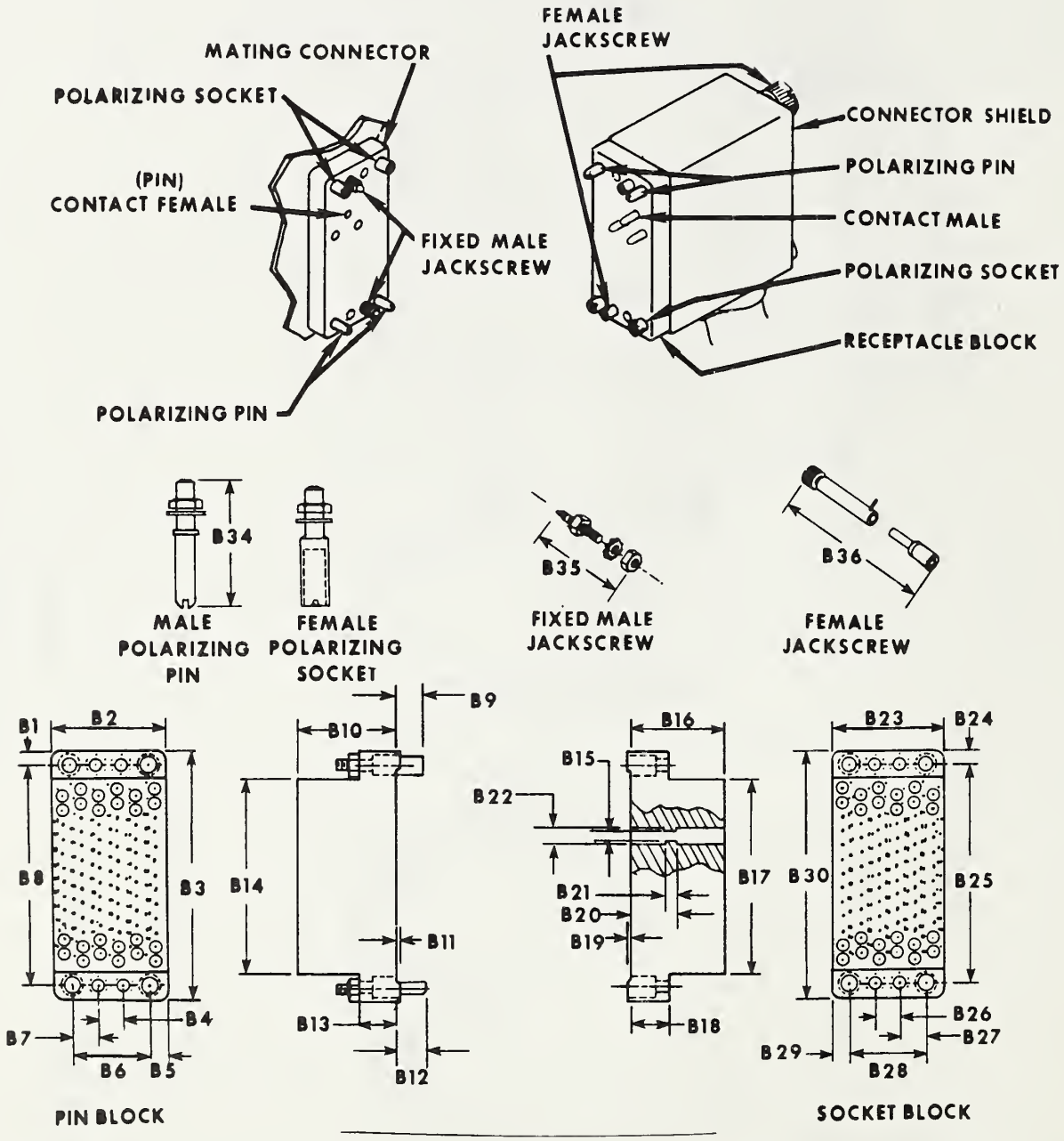
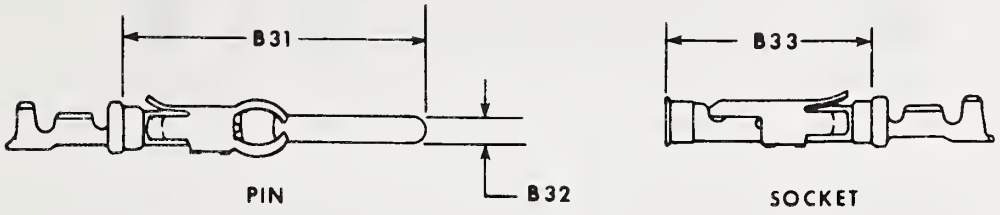
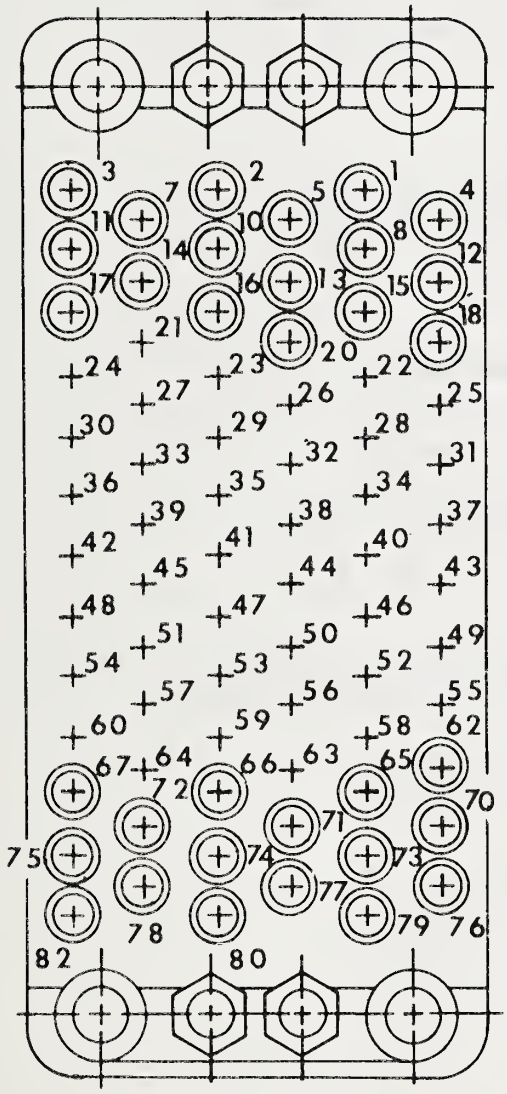


Fig. 3
CONTROL Round Cable Connectors



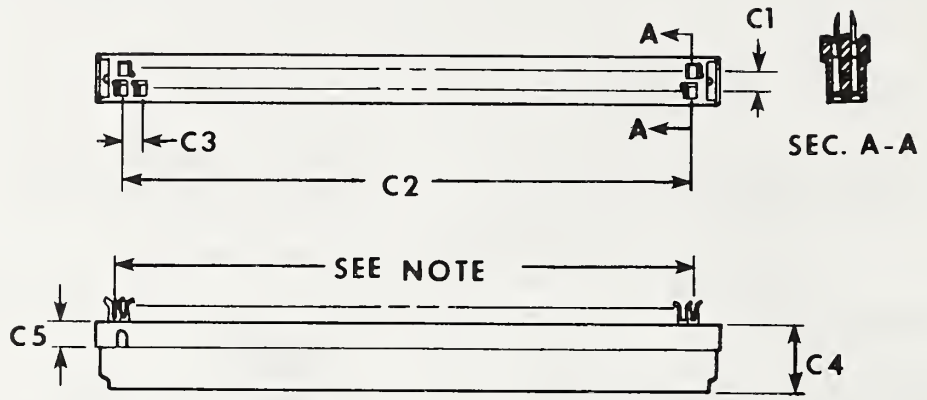


Dimensions	Inches	Millimeters
b_1	0.156	3.96
b_2	1.110	28.19
b_3	2.595	65.91
b_4	0.235	5.97
b_5	0.172	4.37
b_6	0.785	19.93
b_7	0.265	6.73
b_8	2.281	57.94
b_9	0.915	23.24
b_{10}	0.157	3.99
b_{11}	0.011*	0.28*
b_{12}	0.192	4.88
b_{13}	0.365	9.27
b_{14}	1.983	50.37
b_{15}	0.115	2.92
b_{16}	0.915	23.24
b_{17}	1.983	50.37
b_{18}	0.365	9.27
b_{19}	0.011*	0.28*
b_{20}	0.554	14.07
b_{21}	0.054	1.37
b_{22}	0.129	3.28
b_{23}	1.110	28.19
b_{24}	0.156	3.96
b_{25}	2.281	57.94
b_{26}	0.235	5.97
b_{27}	0.265	6.73
b_{28}	0.766	19.46
b_{29}	0.172	4.37
b_{30}	2.595	65.91
b_{31}	0.797	20.24
b_{32}	0.062†	1.57†
b_{33}	0.529	13.44
b_{34}	0.830	21.08
b_{35}	0.815	20.70
b_{36}	2.305	58.55

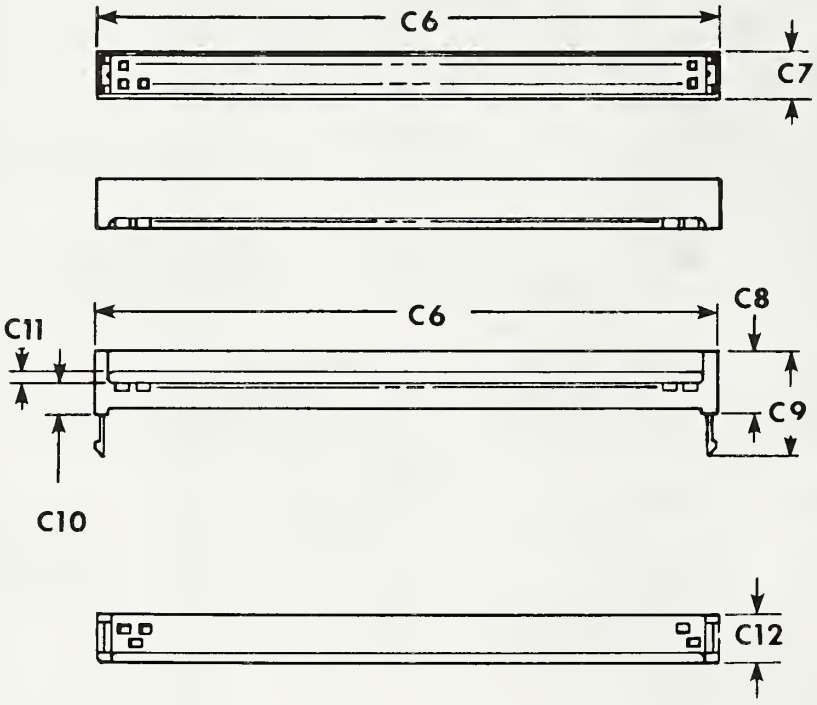
*Typical
†Diameter

NOTE: Circuit identification for pin block. Socket block identification is mirror image.

Fig. 3 – *Continued*

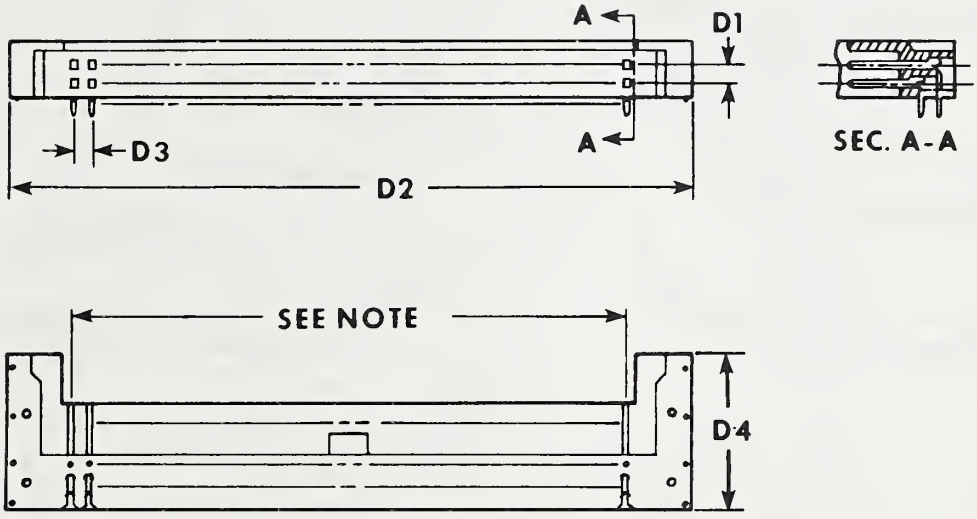


NOTE: 60 contacts on 0.050 inch (1.27 mm) staggered spacing = 2.950 inches (74.93 mm)

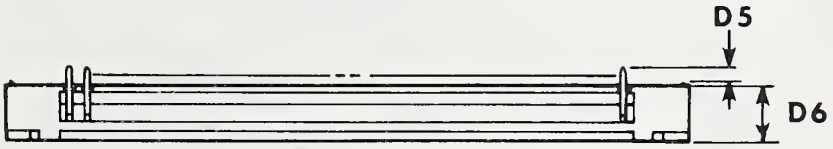


Dimensions	Inches	Millimeters
c_1	0.100	2.54
c_2	2.900	73.66
c_3	0.100	2.54
c_4	0.392	9.96
c_5	0.130	3.30
c_6	3.180	80.77
c_7	0.240	6.10
c_8	0.312	7.92
c_9	0.531	13.49
c_{10}	0.150	3.81
c_{11}	0.050	1.27
c_{12}	0.240	6.10

Fig. 4
CONTROL Flat Cable Plug



NOTE: 60 contacts on 0.100 inch (2.54 mm) spacing = 2.90 inches (73.66 mm)



Dimensions	Inches	Millimeters
d_1	0.100	2.54
d_2	3.580	90.93
d_3	0.100	2.54
d_4	0.810	20.57
d_5	0.092	2.34
d_6	0.295	7.49

Fig. 5
CONTROL Flat Cable Receptacle

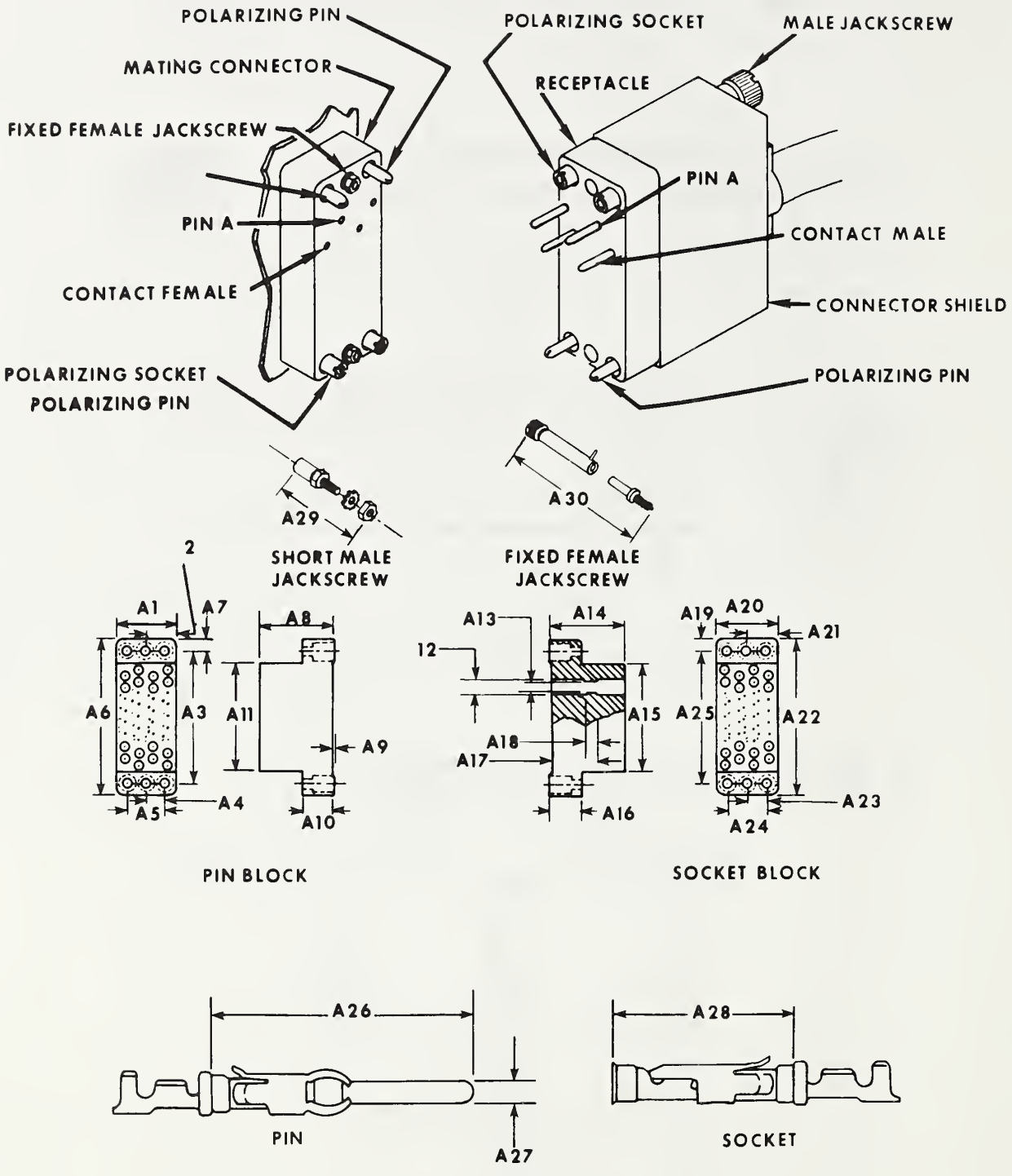
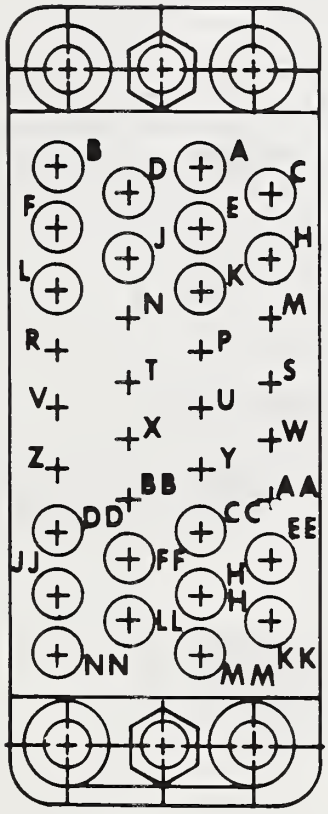


Fig. 6
READ/WRITE Round Cable Connectors

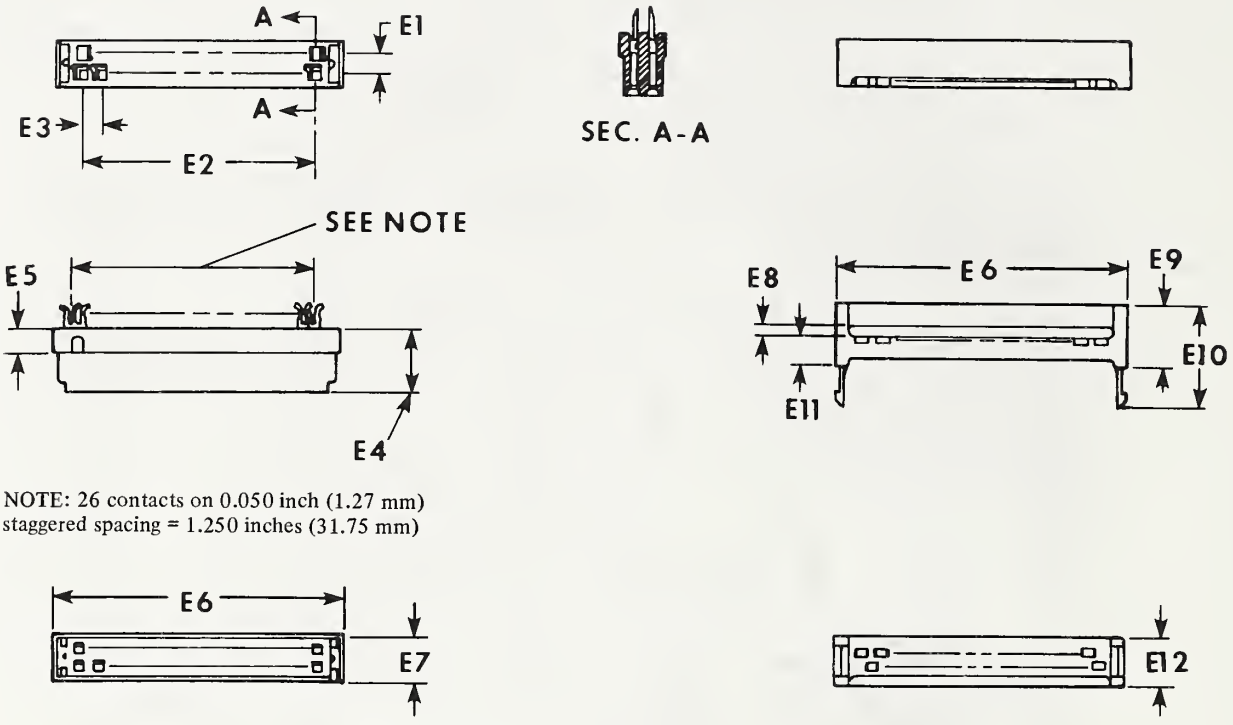


NOTE: Cavity identification for pin block.
Socket block identification is mirror image.

Dimensions	Inches	Millimeters
a_1	0.750	19.05
a_2	0.375	9.53
a_3	1.687	42.85
a_4	0.234	5.94
a_5	0.468	11.89
a_6	2.000	50.80
a_7	0.157	3.99
a_8	0.915	23.24
a_9	0.011*	0.28*
a_{10}	0.365	9.27
a_{11}	1.409	35.79
a_{12}	0.129	3.28
a_{13}	0.115	2.92
a_{14}	0.915	23.24
a_{15}	1.409	35.79
a_{16}	0.365	9.27
a_{17}	0.554	14.07
a_{18}	0.054	1.37
a_{19}	0.157	3.99
a_{20}	0.750	19.05
a_{21}	0.375	9.53
a_{22}	2.000	50.80
a_{23}	0.234	5.94
a_{24}	0.468	11.89
a_{25}	1.687	42.85
a_{26}	0.797	20.24
a_{27}	0.062†	1.57†
a_{28}	0.529	13.44
a_{29}	1.643	41.73
a_{30}	0.837	21.26

*Typical
†Diameter

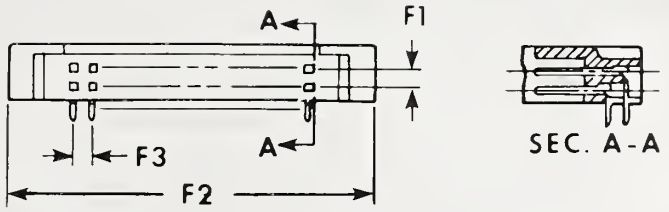
Fig. 6 – *Continued*

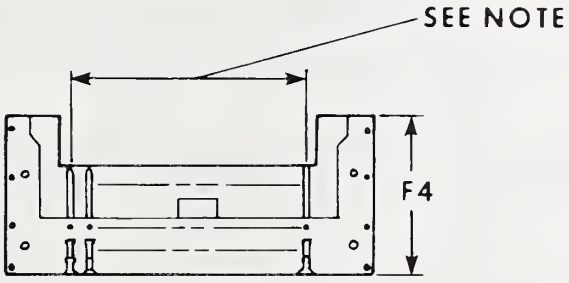


NOTE: 26 contacts on 0.050 inch (1.27 mm) staggered spacing = 1.250 inches (31.75 mm)

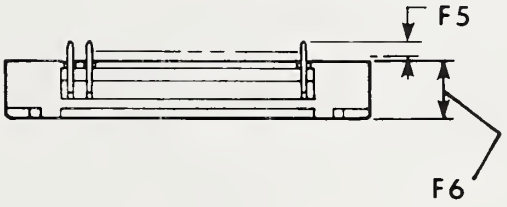
Dimensions	Inches	Millimeters
e_1	0.100	2.54
e_2	1.200	30.48
e_3	0.100	2.54
e_4	0.329	8.36
e_5	0.130	3.30
e_6	1.480	37.59
e_7	0.240	6.10
e_8	0.050	1.27
e_9	0.321	8.15
e_{10}	0.531	13.49
e_{11}	0.150	3.81
e_{12}	0.240	6.10

Fig. 7
READ/WRITE Flat Cable Plug



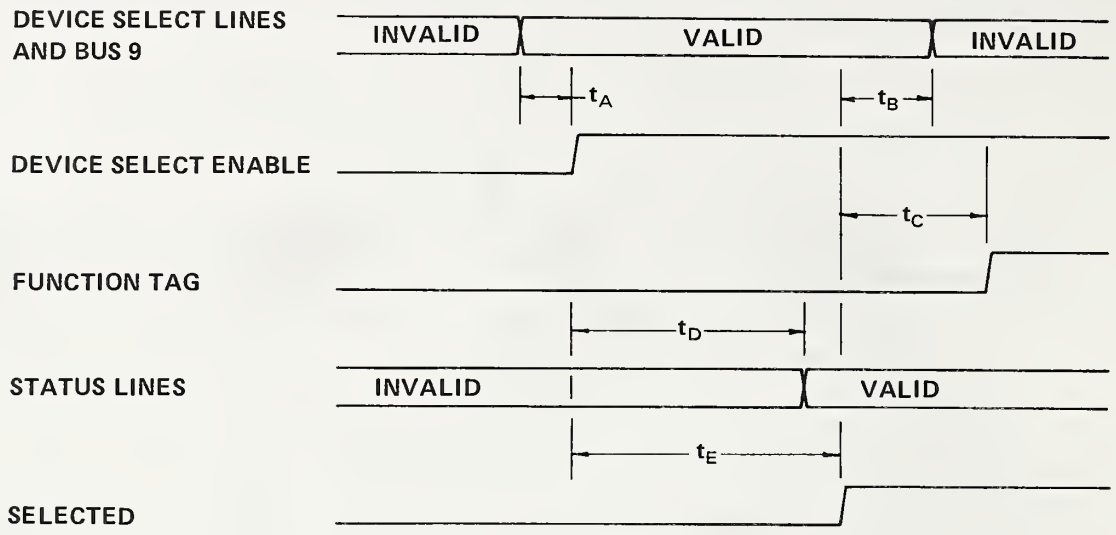


NOTE: 26 contacts on 0.100 inch (2.54 mm) spacing = 1.200 inches (30.48 mm)



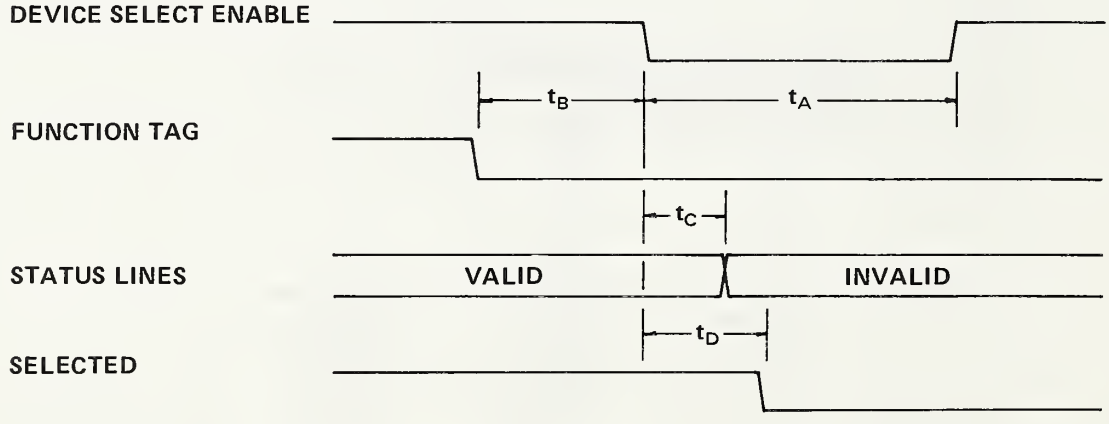
Dimensions	Inches	Millimeters
f_1	0.100	2.54
f_2	1.880	47.75
f_3	0.100	2.54
f_4	0.810	20.57
f_5	0.092	2.34
f_6	0.295	7.49

Fig. 8
READ/WRITE Flat Cable Receptacle



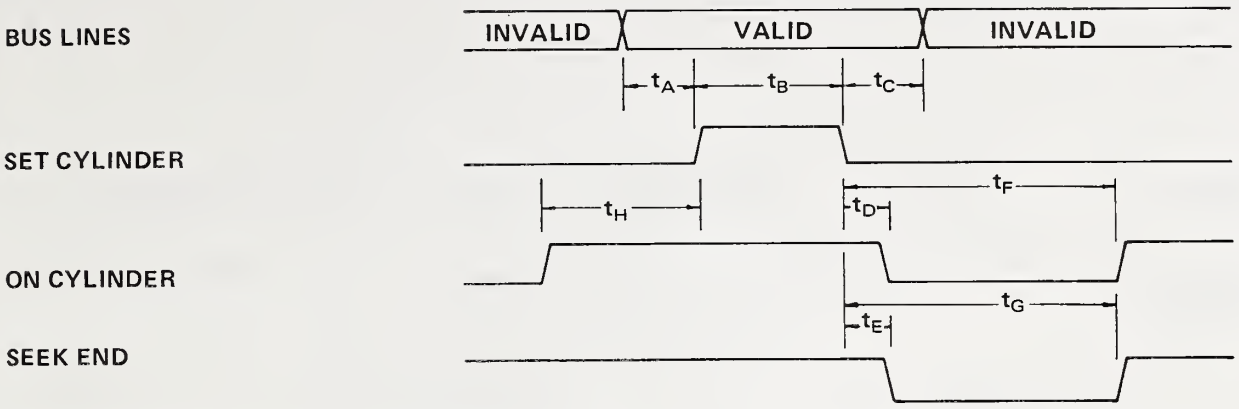
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0.5	–	–	Microseconds
t_B	–	0.5	–	–	Microseconds
t_C	–	1.0	–	–	Microseconds
t_D	–	–	–	1.0	Microseconds
t_E	–	–	–	1.0	Microseconds

Fig. 9
Device Selection Sequence



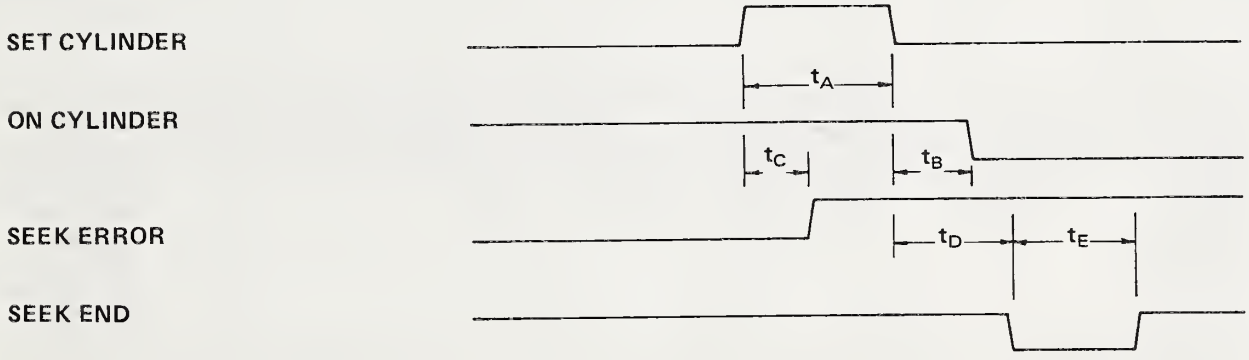
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	1.0	–	–	Microseconds
t_B	–	0.5	–	–	Microseconds
t_C	–	0	–	1.0	Microseconds
t_D	–	–	–	1.0	Microseconds

Fig.10
Device Deselection Sequence



Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0.5	–	–	Microseconds
t_B	–	1.0	–	500	Microseconds
t_C	–	0.5	–	–	Microseconds
t_D	–	–	–	0.5	Microseconds
t_E	–	–	–	0.5	Microseconds
t_F	–	4.0	–	–	Microseconds
t_G	–	4.0	–	–	Microseconds
t_H	–	0.5	–	–	Microseconds

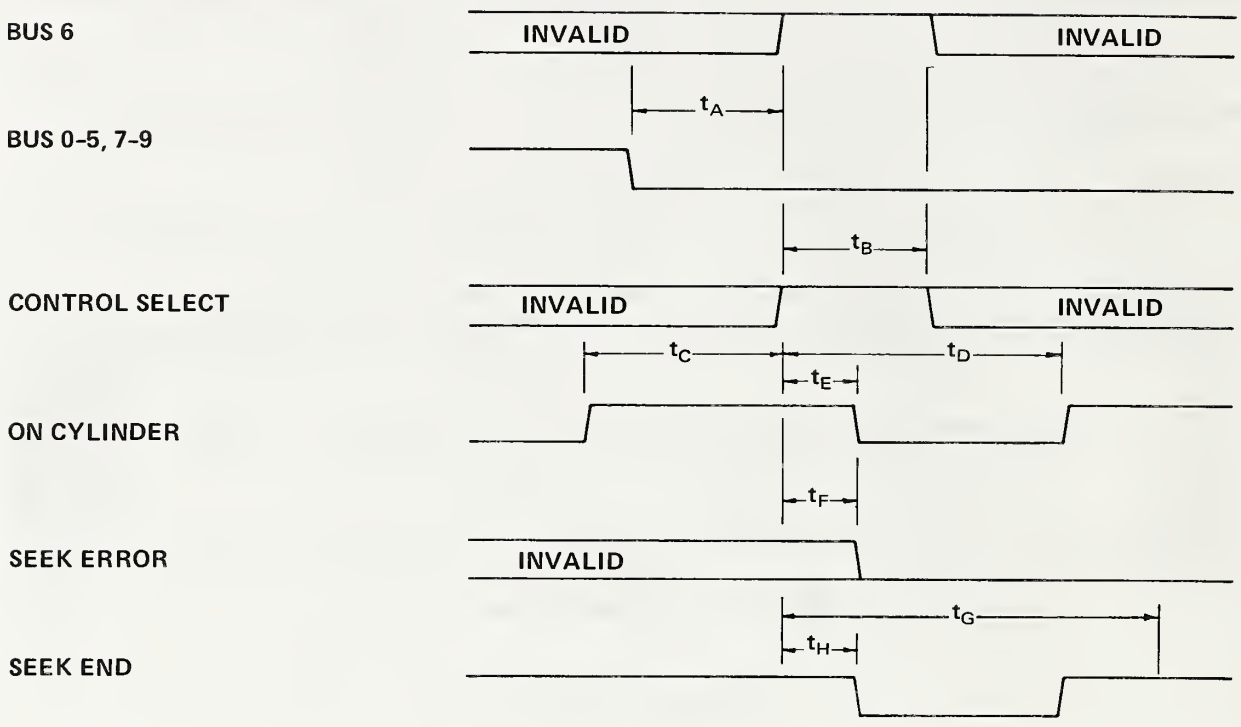
(a) Valid Cylinder Address



Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	1.0	–	500	Microseconds
t_B	–	–	–	0.5	Microseconds
t_C	–	–	–	450	Microseconds
t_D	–	–	–	0.5	Microseconds
t_E	–	4.0	–	–	Microseconds

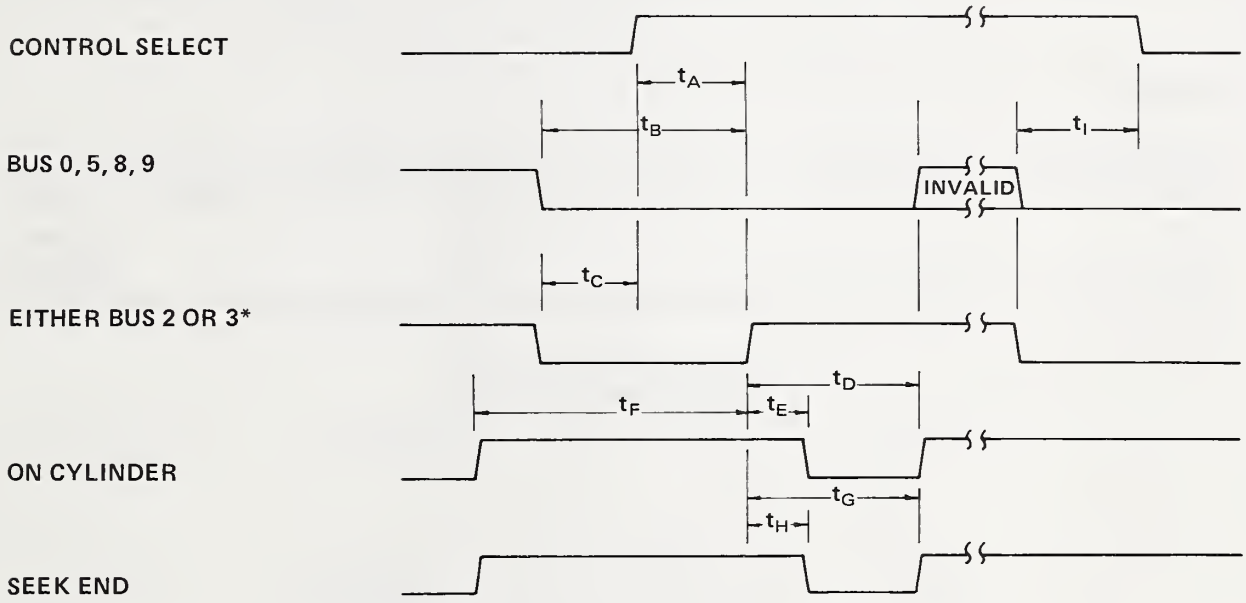
(b) Invalid Cylinder Address

Fig. 11
SEEK Command Sequence



Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0.5	–	–	Microseconds
t_B	"LOGICAL AND" of CONTROL SELECT and BUS 6	1.0	–	500	Microseconds
t_C	–	0.5	–	–	Microseconds
t_D	–	1.0	–	–	Microseconds
t_E	–	–	–	0.5	Microseconds
t_F	–	–	–	0.5	Microseconds
t_G	–	10.0	–	–	Microseconds
t_H	–	–	–	0.5	Microseconds

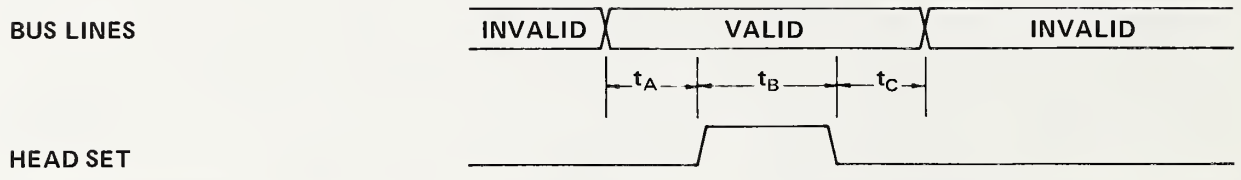
Fig. 12
REZERO Command Sequence



*See 4.1.1.3.3(3) and 4.1.1.3.3(4).

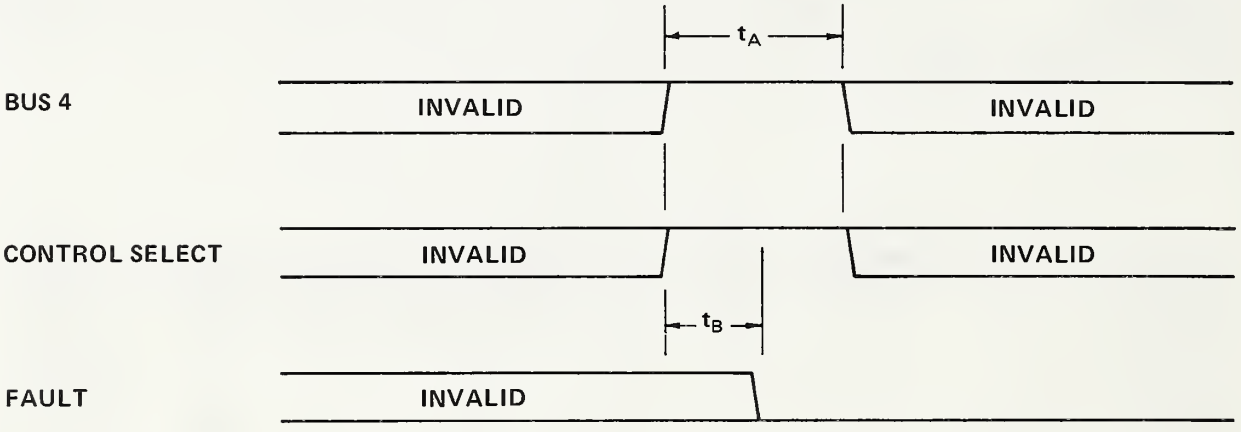
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0	–	–	Microseconds
t_B	–	0.5	–	–	Microseconds
t_C	–	0.5	–	–	Microseconds
t_D	–	–	–	10K	Microseconds
t_E	–	–	–	0.5	Microseconds
t_F	–	0.5	–	–	Microseconds
t_G	–	–	t_D	–	Microseconds
t_H	–	–	–	0.5	Microseconds
t_I	–	0	–	–	Microseconds

Fig. 13
OFFSET Command Sequence



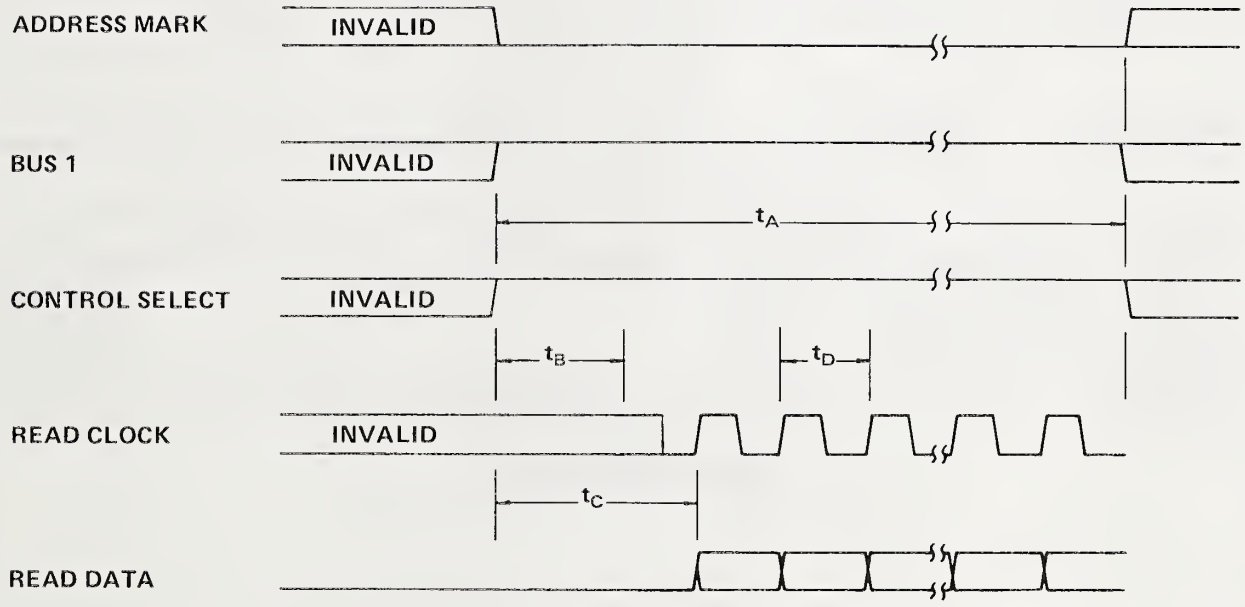
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0.5	–	–	Microseconds
t_B	–	1.0	–	–	Microseconds
t_C	–	0.5	–	–	Microseconds

Fig. 14
HEAD SET Command Sequence



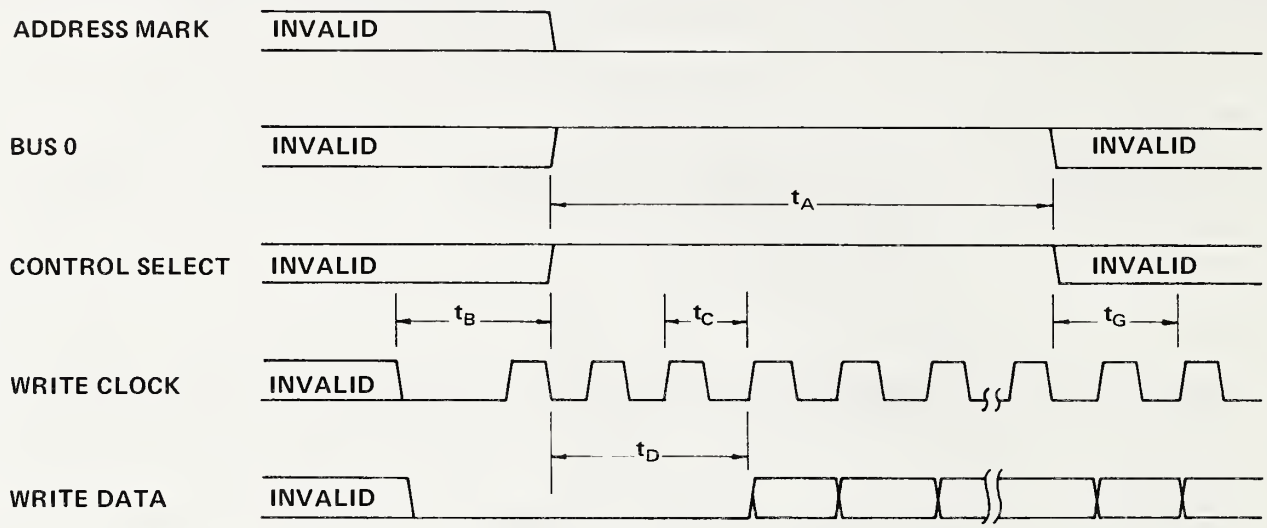
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	"LOGICAL AND" of CONTROL SELECT and BUS 4	0.5	–	–	Microseconds
t_B	–	–	–	0.5	Microseconds

Fig. 15
FAULT CLEAR Command Sequence



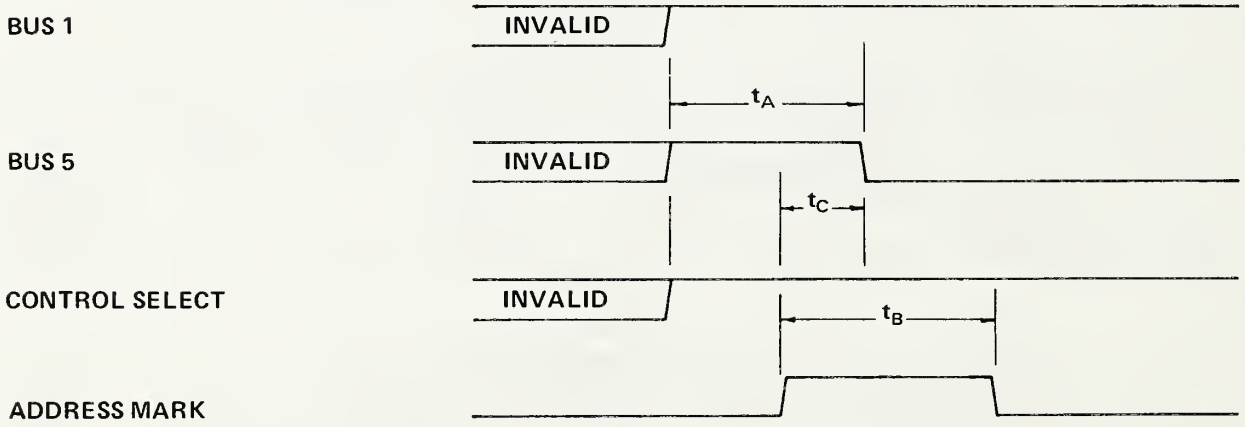
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	"LOGICAL AND" of CONTROL SELECT BUS 1	0	–	–	Microseconds
t_B	Synchronization interval	–	–	9	Microseconds
t_C	Zeroes field	$>t_B$	–	–	Microseconds
t_D	T_P = Nominal bit period	–	T_P	–	Microseconds

Fig. 16
READ Command Sequence



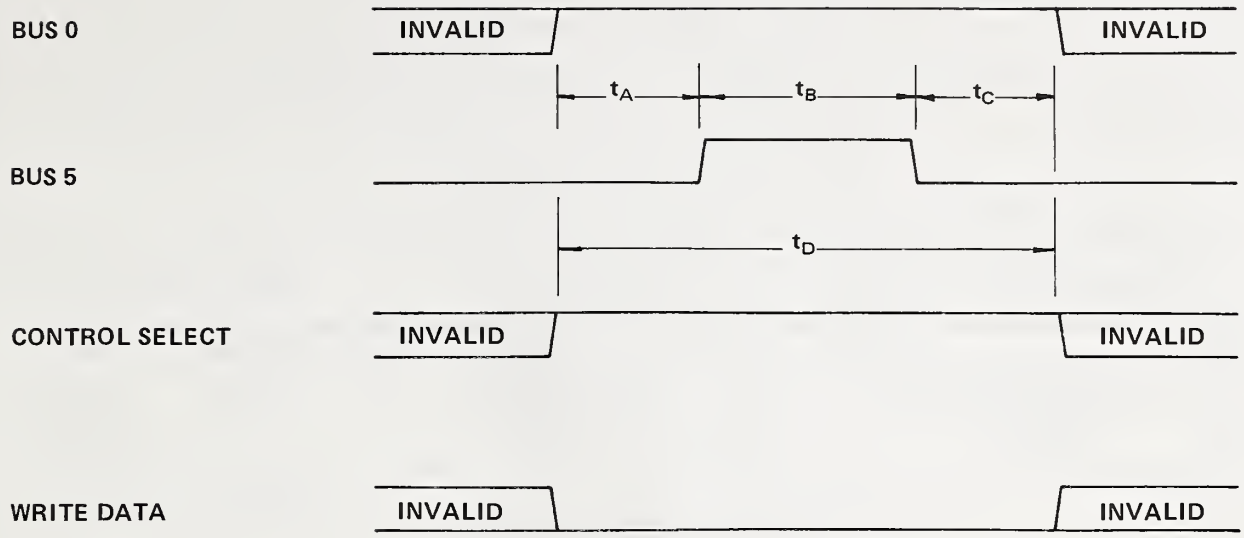
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	"LOGICAL AND" of CONTROL SELECT and BUS 0	0	–	–	Nanoseconds
t_B	–	$2T_P$	–	–	Nanoseconds
t_C	T_P = Nominal bit period	–	T_P	–	Nanoseconds
t_D	Synchronization interval	9	–	–	Microseconds
t_G	–	$3T_P$	–	–	Nanoseconds

Fig. 17
WRITE Command Sequence



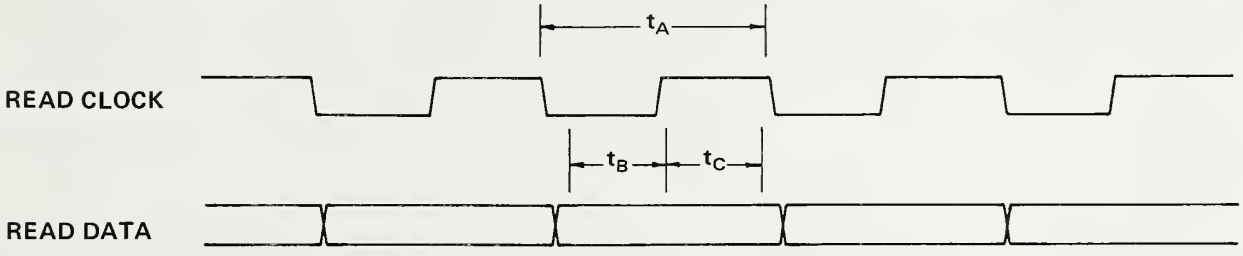
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	"LOGICAL AND" of CONTROL SELECT, BUS 1, BUS 5	0	–	–	Microseconds
t_B	–	1.0	–	–	Microseconds
t_C	–	0	–	1.1	Microseconds

Fig. 18
READ ADDRESS MARK Command Sequence



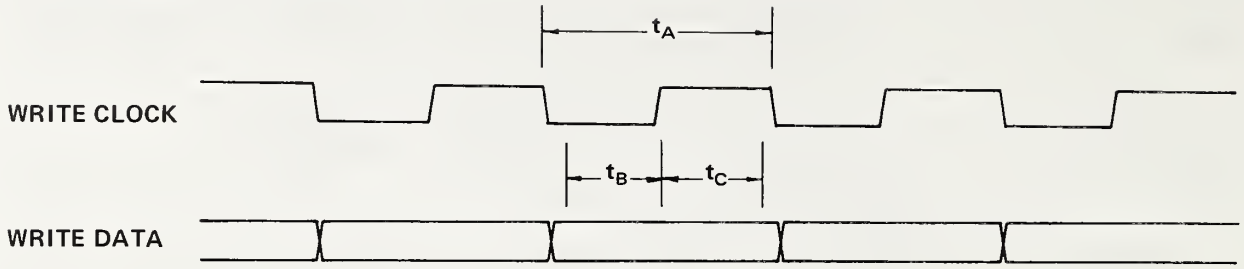
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	5.0	–	–	Microseconds
t_B	T_P = Nominal bit period	$24T_P$	–	$28T_P$	Microseconds
t_C	–	$8T_P$	–	–	Microseconds
t_D	"LOGICAL AND" of CONTROL SELECT, BUS 0	–	–	–	Microseconds

Fig. 19
WRITE ADDRESS MARK Command Sequence



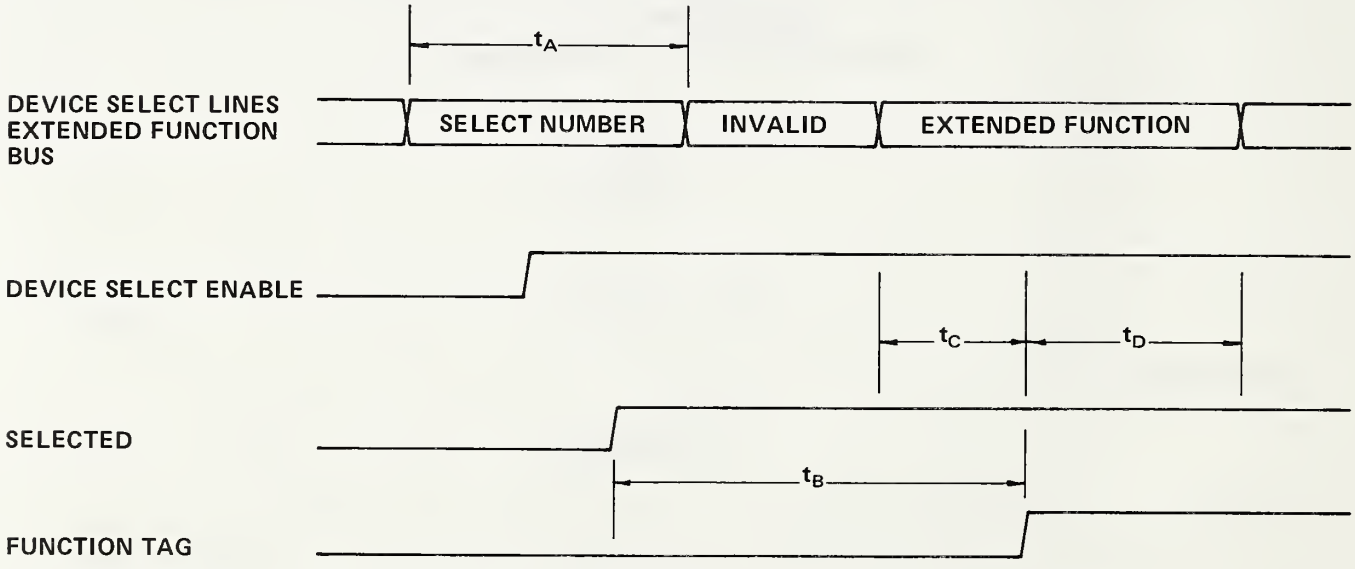
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	T = Nominal bit period	$0.95T_P$	T_P	$1.05T_P$	–
t_B	Set-up time	30	–	–	Nanoseconds
t_C	Hold time	30	–	–	Nanoseconds

Fig. 20
READ CLOCK and READ DATA



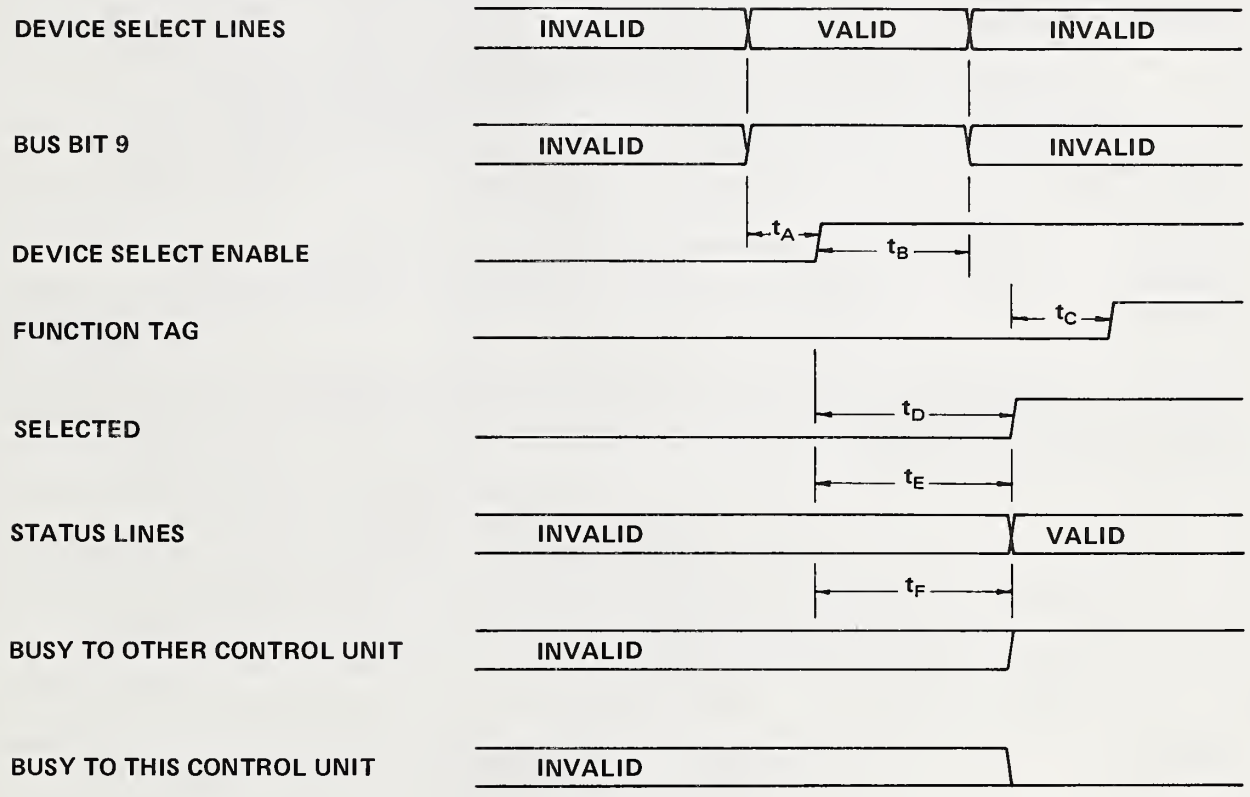
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	T = Nominal bit period	$0.95T_P$	T_P	$1.05T_p$	–
t_B	Set-up time	30	–	–	Nanoseconds
t_C	Hold time	30	–	–	Nanoseconds

Fig. 21
WRITE CLOCK and WRITE DATA



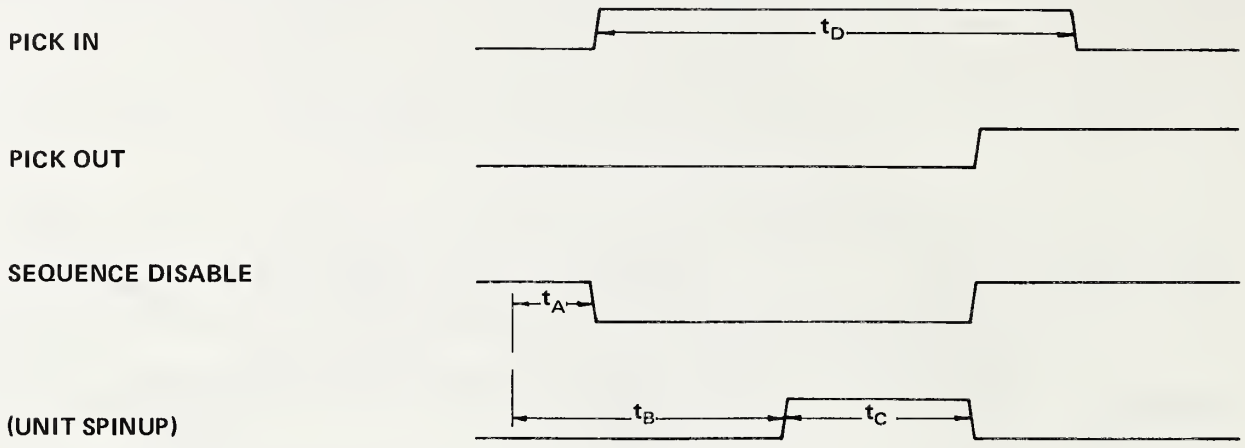
Reference	Comments	Minimum	Typical	Maximum	Units
t_A	See 5.1	–	–	–	Microseconds
t_B	Selected to any function tag	1.0	–	–	Microseconds
t_C	Set-up time	0.5	–	–	Microseconds
t_D	Hold time	0.5	–	–	Microseconds

Fig. 22
Extended Functions



Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0.5	–	–	Microseconds
t_B	–	0.5	–	–	Microseconds
t_C	–	0.5	–	–	Microseconds
t_D	–	–	–	1.0	Microseconds
t_E	–	–	–	1.0	Microseconds
t_F	–	–	–	1.0	Microseconds

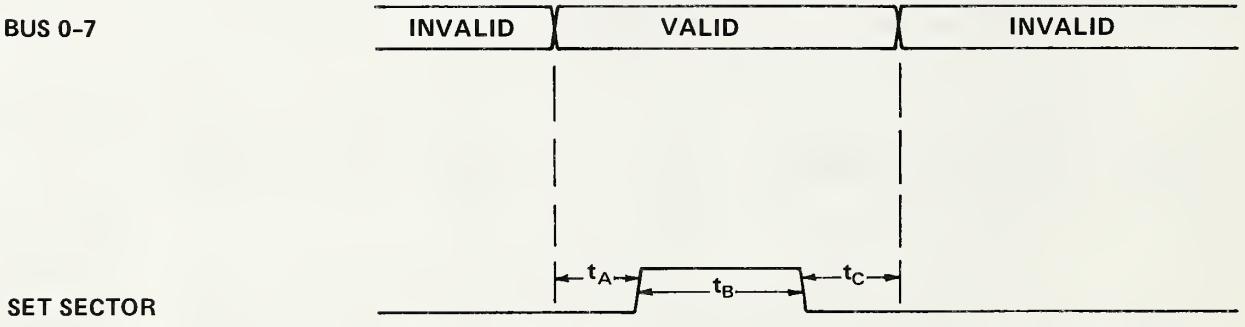
Fig. 23
Dual Port PRIORITY SELECT Command Sequence



Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	1.0	–	–	Microseconds
t_B	–	10.0	–	–	Microseconds
t_C	–	–	1.0	–	Minutes
t_D	–	Sum	–	–	See note

NOTE: The sum of t_B and t_C for all units on a string.

Fig. 24
Spinup Sequencing



Reference	Comments	Minimum	Typical	Maximum	Units
t_A	–	0.5	–	–	Microseconds
t_B	–	1.0	–	–	Microseconds
t_C	–	0.5	–	–	Microseconds

Fig. 25
ROTATIONAL POSITION SENSING

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American National Standards

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NIST-772
(REV. 10-88)

U.S. DEPARTMENT OF COMMERCE
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY

FIPS PUBLICATION CHANGE NOTICE

CHANGE NUMBER 2 - FIPS 60-2 & 62
1-FIPS 61-1,63-1,97,111,130&131

DATE OF CHANGE
1990 December 26

FIPS PUBLICATION NUMBER
See above.

PUBLICATION TITLE FIPS 60-2, I/O Channel Interface; 62, Operational Specifications for Magnetic Tape Subsystems; 61-1, Channel Level Power Control Interface; 63-1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems; 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems; 111, Storage Module Interfaces (w/extens. for enhanced storage module interface); 130, Intelligent Peripheral Interface (IPI); 131, Small Computer System Interface (SCSI).

THIS OFFICE HAS A RECORD OF YOUR INTEREST IN RECEIVING CHANGES TO THE ABOVE FIPS PUBLICATION. THE CHANGE(S) INDICATED BELOW HAVE BEEN PROVIDED BY THE MAINTENANCE AGENCY FOR THIS PUBLICATION AND WILL BE INCLUDED IN THE NEXT PUBLISHED REVISION TO THIS FIPS PUBLICATION. QUESTIONS OR REQUESTS FOR ADDITIONAL INFORMATION SHOULD BE ADDRESSED TO THE MAINTENANCE AGENCY:

Department of Commerce
National Institute of Standards and Technology
National Computer Systems Laboratory
Gaithersburg, MD 20899

CHANGE ITEM(S)

Attached is a reprint from the December 18, 1990, FEDERAL REGISTER (55 FR 51941) which provides approved revisions by the Secretary of Commerce to the FIPS family of input/output interface standards, and the approved discontinuation of the Exclusion and Verification Lists for these standards.

These approved revisions became effective on December 18, 1990, and become an integral part of FIPS 60-2, 61-1, 62, 63-1, 97, 111, 130 and 131, and, as such, are considered to be included whenever reference is made to them.

These approved revisions should be filed with each FIPS listed above.

Attachment

Copies of FIPS are available from:

National Technical Information Service (NTIS)
ATTN: Sales Office, Sills Building
5285 Port Royal Road
Springfield, Virginia 22161

Phone - 703/487-4650 Office Hours - 7:45 a.m. to 4:15 p.m.

ELECTRONIC FORM

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Vol. 55 No. 243
Pages 51895-52036

Federal Register

Tuesday
December 18, 1990

National Institute of Standards and Technology

[Docket No. 900101-0219]

RIN 0693-AA59

Approval of Revisions to Federal Information Processing Standards (FIPS) Family of Input/Output Interface Standards

AGENCY: National Institute of Standards and Technology (NIST), Commerce.
ACTION: The purpose of this notice is to announce that the Secretary of Commerce has approved revisions to the Federal Information Processing Standards (FIPS) family of input/output interface standards, and has approved discontinuation of the exclusion and verification lists for these standards.

SUMMARY: On March 20, 1990, notice was published in the Federal Register (55 FR 10272) proposing revision of Federal Information Processing Standards (FIPS) 60-2, 61-1, 62, 63-1, 97, 111, 130, and 131 to make them non-mandatory, and discontinue the exclusion and verification lists for these standards. This proposal superseded the proposal for revision of these standards announced in the Federal Register (52 FR 44462) of November 19, 1987. Procedures for the Exclusion List for FIPS 60, 61, 62, 63, and 97 were published in the Federal Register on

September 3, 1982 (47 FR 38959–38960). Procedures for the Verification List for FIPS 60, 61, 62, 63, and 97 were published in the Federal Register on December 11, 1979 (44 FR 71444–71445) and on April 7, 1981 (46 FR 20719–20720).

The written comments submitted by interested parties and other material available to the Department relevant to these proposed revisions were reviewed by NIST. On the basis of this review, NIST recommended that the Secretary approve revisions to the input/output family of standards and approve discontinuation of the exclusion and verification lists for these standards. NIST prepared a detailed justification document for the Secretary's review in support of those recommendations.

This notice provides only the changes to the revised standards.

EFFECTIVE DATE: These revisions are effective December 18, 1990.

ADDRESSES: Interested parties may obtain copies of FIPS PUBS 60–2, 61–1, 62, 63–1, 97, 111, 130, and 131 from the National Technical Information Service, U.S. Department of Commerce, Springfield, VA 22161.

FOR FURTHER INFORMATION CONTACT: Ms. Shirley Radack, National Institute of Standards and Technology, Gaithersburg, MD 20899, telephone (301) 975–2833.

SUPPLEMENTARY INFORMATION: Under the provisions of 40 U.S.C. 759(d), the Secretary of Commerce is authorized to promulgate standards and guidelines for Federal computer systems, and to make such standards compulsory and binding to the extent to which the Secretary determines necessary to improve the efficiency of operation, or security and privacy of Federal computer systems.

The family of I/O interface standards currently includes:

a. FIPS 60–2, I/O Channel Interface, revised July 29, 1983.

b. FIPS 61–1, Channel Level Power Control Interface, revised July 13, 1982.

c. FIPS 62, Operational Specifications for Magnetic Tape Subsystems, revised December 30, 1980.

d. FIPS 63–1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems, revised April 14, 1983; Supplement to FIPS PUB. 63–1, Additional Operational Specifications for Variable Block Rotating Mass Storage Subsystems, April 14, 1983.

e. FIPS 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems, February 4, 1983.

f. FIPS 111, Storage Module Interfaces (with extensions for enhanced storage module interfaces), April 18, 1985.

g. FIPS 130, Intelligent Peripheral Interface (IPI), July 16, 1987.

h. FIPS 131, Small Computer System Interface (SCSI) July 16, 1987.

The following revisions are being made effective immediately upon publication. A delayed effective date is not required because these standards are exempt from the Administrative Procedure Act by U.S.C. 553(a)(2).

Revisions to Federal Information Processing Standards 60–2, 61–1, 62, 63–1, 97, 111, 130, and 131.

FIPS 60–2, I/O Channel Interface, is revised as follows:

Applicability. This standard addresses the interconnection of computer peripheral equipment as a part of ADP systems for the following types of peripherals: (1) Magnetic tape equipment employing open reel-to-reel magnetic tape storage devices, specifically excluding magnetic tape cassette and tape cartridge storage devices, (2) magnetic disk storage equipment employing disk drives each having a capacity greater than 7 megabytes per storage module, excluding flexible disk and disk cartridge devices having a smaller storage capacity per device, and (3) other peripheral equipment employing peripheral device types for which operational specifications standards have been issued as Federal Information Processing Standards. This standard is recommended for use in the acquisition of peripheral equipment for ADP systems with input/output channel interfaces as specified in the technical specifications, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective December 13, 1979. The first revision became effective June 23, 1980, and the second revision became effective July 29, 1983. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 61–1, Channel Level Power Control Interface, is revised as follows:

Applicability. This standard addresses the power control interface in connecting computer peripheral equipment to ADP systems. It is recommended for use when FIPS 60–2 is used, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective June 23, 1980, and the first revision became effective July 13, 1982. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 62, Operational Specifications for Magnetic Tape Subsystems, is revised as follows:

Applicability. This standard addresses magnetic tape equipment connected to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such equipment, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective June 23, 1980. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 63–1, Operational Specifications for Variable Block Rotating Mass Storage Subsystems, is revised as follows:

Applicability. This standard addresses peripheral device dependent operational interfaces for connecting variable block rotating mass storage equipment to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such variable block rotating mass storage equipment for connection to ADP systems, when it is determined that interchange of equipment between different systems is likely.

Implementation. This standard became effective June 23, 1980, and the first revision became effective April 14, 1983. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 97, Operational Specifications for Fixed Block Rotating Mass Storage Subsystems, is revised as follows:

Applicability. This standard addresses the peripheral device dependent operational interface specifications for connecting fixed block rotating mass storage equipment to ADP systems through FIPS 60 interfaces. It is recommended for use in the acquisition of such fixed block rotating mass storage equipment for connection to ADP systems, when it is determined that interchange of equipment between different systems is likely.

Implementation. The original version of this standard became effective February 4, 1983. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 111, Storage Module Interfaces, is revised as follows:

Applicability. This standard addresses connection of a disk drive to a controller as part of an ADP system. This standard is recommended for use in the acquisition of disk systems that are

connected to small and medium sized computer systems, when it is determined that interchange of equipment between different systems is likely.

Implementation. This standard became effective May 18, 1985. This revision becomes effective December 18, 1990.

Waivers. This standard is non-mandatory. No waivers are required.

FIPS 130, Intelligent Peripheral Interface (IPI), is revised as follows:

Section 8, Applicability. This standard applies to the connection of computers to storage peripheral device controllers. This standard is recommended for use in the acquisition of magnetic disk drives, optical disk drives, and tape drives to be connected to minicomputer systems, when it is determined that interchange of equipment between different systems is likely.

Section 10, Implementation. This standard became effective December 16, 1987. This revision becomes effective December 18, 1990.

Section 11, Waivers. This standard is non-mandatory. No waivers are required.

FIPS 131, Small Computer System Interface (SCSI) is revised as follows:

Section 8, Applicability. This standard addresses the connection of small computers to peripheral devices with integral controllers. This standard is recommended for use in the acquisition of storage peripherals and small computer systems for office or laboratory use, when it is determined that interchange of equipment between different systems is likely.

Section 10, Implementation. This standard became effective December 16, 1987. This revision becomes effective December 18, 1990.

Section 11, Waivers. This standard is non-mandatory. No waivers are required.

Dated: December 12, 1990.

John W. Lyons,

Director.

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